EPC®-100

Hardware Reference

RadiSys® Corporation

5445 NE Dawson Creek Drive

Hillsboro, OR 97124

Phone: (503) 615-1100

Fax: (503) 615-1150

http://www.radisys.com

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Chapter 1 - Product Description

About this Manual

This manual assumes that the reader has good familiarity with PC sytems based on the Intel x86 architecture and some familiarity with CompactPCI (cPCI) bus architecture.

This manual was written to provide detailed hardware reference information for OEMs, system integrators, and others who use the EPC-100 as a component of their cPCI bus systems. The reader should be able to install the EPC-100 and configure the BIOS based on the information in this manual.

The information in this manual is organized into the following sections:

Front Matter	Table of Contents, List of Figures, List of Tables
Chapter 1	*Introduction*. Provides an introduction to the EPC-100, a brief descripions of the features provided, and a table of specifications.
Chapter 2	*Installation and Configuration*. Covers the details of installing the EPC-100 in a cPCI mainframe and installing driver software.
Chapter 3	*BIOS Configuration*. Describes the process of BIOS configuration using the built-in BIOS setup menus.
Chapter 4	*Theory of Operation*. Describes how the components of the EPC-100 operate to provide an ISA/ cPCI bus compatible embedded computer with standard PC peripherals and a PCI interface.
Chapter 5	*Service and Support*. Describes how to obtain technical support and service from RadiSys Corp.

Appendix A *Chipset and I/O Map*. Maps the addresses used for I/O and by the chipset registers.

Appendix B *Interrupts and DMA Channels*. Shows the DMA channel and IRQ assignments to the peripherals supported by the EPC-100.

Appendix C *Connector*s. Details the location, form, and pin-outs of the connectors used in the EPC-100.

Appendix D *Error Messages and Diagnosis*. Explanations of common error messages and start-up codes.

Overview

The EPC-100 is a highly integrated PC-compatible computer designed for use in the full 32-bit CompactPCI (cPCI) bus environment. The EPC-100 is a two-slot 6U cPCI bus module that supports up to seven 3U/6U cPCI peripheral slots via a DEC 21150 PCI-PCI bridge chip. It is compatible with all major PC software environments, including Microsoft DOS, Microsoft Windows 95, and NT 4.0, and IBM OS/2, plus others.

The PC-compatible portion of the architecture includes the following PC-standard features:

- Intel Pentium 100, 133, 166, or 200 MHz processors.
- 256 KB secondary (L2) cache (512KB optional).
- 8, 16, 32, 64, 128, or 256 MB of memory, using dual 72-pin socket SODIMM DRAM.
- Two EIDE channels drive four devices through on-board headers with no external power required.
- Desktop power management compliant with the APM 1.1 specification.
- System BIOS support for Plug-and-Play peripherals is compliant with the 1.0a PnP BIOS specification.
- Tested compatibility with the Microsoft Windows NT 4.0 Workstation Hardware Compatibility Test (HCT). The EPC-100 will be listed in the Hardware Compatibility List (HCL).
- All other standard PC architectural features, including an on-board speaker.
- Phoenix NuBIOS with RadiSys enhancements to support the additional on-board features and cPCI bus environment.

Product Description

Standard front panel PC peripheral interfaces with standard interface connectors include:

- two RS232 serial ports
- a bi-directional IEEE 1284 ECP/EPP parallel port
- two USB ports
- a fast SCSI-II controller with front panel interface
- 10/100BaseTX and 10BASE2 Ethernet ports
- PS/2 style mouse and keyboard connectors

Additional features include:

- SVGA interface. This PCIbus interface is based on the Cirrus Logic CL-GD5446 chip, with up to 4MB of video RAM providing local bus graphics performance and resolutions up to 1280x1024, with 64K colors. The standard 15-pin connector for this port is enhanced with a programmable output on pin 15, which is not connected on a standard VGA interface.
- 10BASE2 and 10/100Base-TX Ethernet interfaces. The interface is based on the Digital 21143 Ethernet controller. Interface configuration (Emulation mode and address/interrupt control) is software controlled.
- A watchdog timer. This device can be configured to generate an IRQ9 interrupt and either halt or perform a warm reboot of the processor, depending on a BIOS setup option. The timer is implemented as a software-retriggerable one-shot, with a programmable reset interval ranging from 128 ms to 8.2 sec.
- Optional on-board 2.5" ATA hard drive.

cPCI bus

The cPCI bus is accessed from the EPC-100's PCI bus via a DEC 21150 PCI-PCI bridge. This bridge connects the onboard PCI bus (bus 0) with the mainframe's cPCI bus (bus 1), which may have as many as seven additional cPCI devices connected to it. This is described in the following sections covering the system controller functions and the interface to cPCI devices.

The cPCI standard was developed by a consortium of manufacturers known as the PCI Industrial Computer Manufacturers Group (PICMG). For further information

about PICMG and the cPCI standard consult the PICMG website at http://www.picmg.org.

cPCI Device Interface

The EPC-100 implements a 32 bit CompactPCI system slot board capable of driving seven CompactPCI slots. A DEC 21150 PCI-PCI bridge chip is used to interface between the base board's local PCI bus and the CompactPCI bus. The bridge chip controls a layer of buffers between it and the CompactPCI bus and has a glueless interface to the local PCI bus. PCI interrupts (INT[A:D]#) are directly handled by the CPU sub-module's interrupt controller.

The CompactPCI bus interface uses the standard 2 mm-pitch, 7-row Hard Metric connector. This connector has a 7 column by 47 row array of pins divided into two groups corresponding to the physical implementation. The two outside columns are used as a ground shield for EMI protection. Of the remaining columns, J1 pins 1-25 provide 32 bit PCI and connector keying implemented as one connector. J2 pins 1-22 provide 64 bit support, clocking, and arbitration with a portion reserved for future use.

The CompactPCI bus interface includes the following features:

- The DEC 21150 PCI-PCI bridge provides full CompactPCI bus System Controller (Slot 1) features including bus arbitration, signal pull-ups, device configuration, idle bus parking, and clock generation and buffering.
- Support for CompactPCI Signal Additions (to the PCI specification): push-button reset, power supply status, system slot identification, and separate primary and secondary interrupts.
- The EPC-100 presents a double load on each CompactPCI bus signal as allowed by the CompactPCI standard.

Specifications

Environmental Specifications

The following are the environmental specifications for the EPC-100.

Characteristic		Value
Temperature	operating	100MHz: 0-60°C at point of entry of forced air derated 2°C per 1000 ft (300 m) over 6600 ft (2000m) 133MHz: 0-60°C at point of entry of forced air derated 2°C per 1000 ft (300 m) over 6600 ft (2000m) 166MHz: 0-45°C at point of entry of forced air derated 2°C per 1000 ft (300 m) over 6600 ft (2000m) 200MHz: 0-40°C at point of entry of forced air derated 2°C per 1000 ft (300 m) over 6600 ft (2000m) 2°C per hour max excursion gradient
	storage	-40°C - 85°C 5°C per hour max excursion gradient
Humidity	operating	5% - 95% noncondensing
	storage	5% - 95% noncondensing
Altitude	operating	0 - 10,000 ft (3000 m)
	storage	0 - 40,000 ft (12,000 m)
Airflow	operating	300 LFPM, (Linear Feet Per Minute)
----continued----		

Table 1-1. EPC-100 Environmental Specifications.

Vibration	operating	2.5 g acceleration over 5-300 Hz sine wave, 1 oct/min sine sweep
without HDD	storage	5 g acceleration over 5-2K Hz sine wave, 1 oct/min sine sweep
Shock	operating	30 g, 11 ms duration, half-sine shock pulse
without HDD	storage	50 g, 11 ms duration, half-sine shock pulse
Vibration	operating	0.5mm P-P (5 - 22 Hz) 0.5G (max.) (22 - 400 Hz)
with HDD	storage	5mm P-P (5 - 22 Hz) 5G (max.) (22 - 400 Hz)
Shock	operating	1470m/s^2 (150G) (2ms half sine wave)
with HDD	storage	2450m/s^2 (250G) (2ms half sine wave)

Table 1-1 (continued). EPC-100 Environmental Specifications

Other Specifications

The following table contains additional specifications. A typical system is assumed, with SVGA and 32 MB of RAM.

Characteristic		Value
Electrical TBD		
Current	+5V	2.6A. typical, depending on processor
	+12V	0.1A typical
	+3.3V	3.1A typical, EPC100-100 3.2A typical, EPC 100-133 5.4A typical, EPC-100-166 3.4A typical, EPC-100-200MT
	-12V	0.2A typical
Mechanical		
	Weight	2.7 lb. (1.3 kg)
	Dimensions	see cPCI Specification Rev. 1.0 for a 6U 2-slot module.
Safety		
	UL 1244 (not tested)	
	IEC 1010.1 (1990) Incl. Amend 1 (1992)/EN61010 (1993)	
	CSA C22. #1010.1 (1992) (not tested)	

Table 1-2. Additional EPC-100 Specifications.

EMC	
	CE Mark
	CISPR 11:1990/EN 55011(1991): Group 1 Class A
	IEC 801-2:1991/EN50082-1 (1992): 4kV CD, 8kV AD
	IEC 801-3:1984/EN50082-1 (1992): 3V/m
	IEC 801-4:1988/EN50082-1 (1992): 1kV Power Line
	Low Voltage Directive 89/336/EEC

Table 1-2. Additional EPC-100 Specifications. (cont'd)

Chapter 2 - Installation

Introduction

This chapter tells you how to install the EPC-100 in a Compact PCI (cPCI) chassis.

There are three user-configurable jumpers. One enables/disables the CPU fan failure test during Power On Self-test (POST). The second enables/disables the SCSI termination, so that the EPC-100 can be used as any element in a SCSI daisy-chain. The third jumper determines whether an external floppy disk drive will be powered by the on-board floppy drive connector or not. These jumpers are described in *Appendix C- Connectors and Jumpers*.

You will also need to install device drivers for the SVGA video adapter and the Ethernet adapter. These procedures are described in *System Software Installation* in this chapter.

All other setup is done by configuring BIOS options as described in *Chapter 3 - BIOS Configuration*.

⚠ **DO NOT REMOVE THE EPC-100 MODULE FROM ITS ANTI-STATIC BAG UNLESS YOU ARE IN A STATIC-FREE ENVIRONMENT.**

The EPC-100, like most electronic devices, is susceptible to electrostatic discharge (ESD) damage. ESD damage is not always immediately obvious. It can cause a partial breakdown in semiconductor devices that might not result in immediate failure.

⚠ **DURING ALL OF THIS INSTALLATION PROCESS, MAKE SURE THAT POWER TO YOUR SYSTEM IS OFF.**

The EPC-100 is not designed to be inserted or removed while the chassis is powered up.

Inserting the EPC-100

⚠ **WHEN HANDLING OR INSERTING THE EPC-100 MODULE, AVOID TOUCHING THE CIRCUIT BOARD AND CONNECTOR PINS, AND MAKE SURE THE ENVIRONMENT IS STATIC-FREE.**

To install the EPC-100 in the cPCI chassis, make sure that the extractor handles on the front panel are pulled away from each other to their maximum extent. Engage the chassis guides with the EPC-100 and push it in until the extractor handles rest on the latch rail extrusion of the cPCI chassis. Complete the insertion by pressing the extractor handles inwards towards the center of the front panel until the EPC-100 is fully seated in the chassis and the extractor handles lock into place.

Removing the EPC-100

To remove the EPC-100 from the cPCI chassis, press the latch part of the extractors inward until the extractor handle swings out and pivots freely. Then pull outward on the extractor handles until the EPC-100 disengages from the rear connector. Slide the EPC-100 out of the cPCI chassis and place it in the anti-static bag that it came in.

Configuring the EPC-100

Connecting Peripherals to the EPC-100

⚠ **DO NOT PLUG IN ANY CABLE OR CONNECTOR INTO THE FRONT PANEL CONNECTORS WHILE THE SYSTEM IS POWERED UP. ELECTRONICS EQUIPMENT IS GENERALLY NOT DESIGNED TO WITHSTAND FLUCTUATIONS IN POWER. THUS DAMAGE COULD ARISE FROM PLUGGING IN A DEVICE OR BOARD WHILE POWER IS ON. NEVER PLUG IN A SERIAL OR PARALLEL DEVICE, KEYBOARD, TRANSCEIVER, MONITOR OR OTHER COMPONENT WHILE THE SYSTEM IS ON.**

Installation

The next step of installation is connecting peripherals, typically a video display and keyboard, and perhaps a mouse, modem, printer, etc. Pin-outs for the EPC-100 front-panel connectors are specified in *Appendix C - Connector and Jumpers.*

SCSI Termination

When you configure SCSI peripherals to work with the EPC-100, you need to consider the placement of the EPC-100 in the SCSI chain. If the EPC-100 is to be the last device in the SCSI chain, it must be terminated. The SCSI termination jumper placement is described in *Appendix C - Connectors and Jumpers.*

System Software Installation

Operating System Software

The EPC-100 is shipped without operating system software installed on its optional hard disk. To load the operating system software of your choice, use the floppy drive connector located at the rear of the main circuit board to connect a temporary floppy disk drive, then boot from a bootable floppy disk.

⚠ **THE FLOPPY DRIVE CONNECTOR CAN BE CONFIGURED TO SUPPLY POWER TO THE FLOPPY DRIVE VIA THE FLOPPY CABLE. YOUR FLOPPY DRIVE MAY OR MAY NOT REQUIRE THIS. PLEASE REFER TO *FLOPPY POWER JUMPER* IN *APPENDIX C* FOR MORE INFORMATION BEFORE YOU ATTEMPT TO CONNECT A FLOPPY DRIVE.**

You can then use the SCSI-2 connector on the front panel to connect an external SCSI CDROM drive and load the operating system software from it.

Video Driver Software

The video driver software is supplied on a diskette with part number 80-1676-00 labeled Video Drivers, Cirrus Logic CL-GD5446/Windows NT 4.0. If you need to install a different driver for an operating system other than Windows NT 4.0, consult Cirrus Logic at http://www.cirrus.com/support/.

Ethernet Software

The Ethernet driver software is supplied on a diskette with part number 80-1677-00 labeled Ethernet Drivers, DEC 21143/Windows NT 4.0. If you need to install a different driver for an operating system other than Windows NT 4.0, consult Digital Equipment Corporation at http://www.digital.com/info/semiconductor/support.htm.

Chapter 3 - BIOS Configuration

Introduction

The EPC-100 uses the Phoenix NuBIOS to configure and select various system options. This section details the various menus and sub-menus that are used to configure the system. This section is written as though you are setting up each field in sequence and for the first time. Your system may be correctly pre-configured and require very little setup.

Note: If at any time you wish to revert to the original BIOS settings, select Get Default Values from the Exit Menu, described in this chapter. This restores the original BIOS settings.

Some error messages might occur during the execution of the BIOS initialization sequence. If errors occur during the power-on self-test (POST), the BIOS will display the error on the appropriate line of the screen display and, depending on how your system is configured, will either pause or attempt to continue. Refer to *Appendix D - Error Messages & Diagnosis.*

BIOS Setup Screens

The EPC-100's BIOS contains a setup function to display and modify the system configuration. This information is maintained in the EPC-100's nonvolatile CMOS RAM and is used by the BIOS to initialize the EPC-100 hardware.

The BIOS Setup can only be entered during the system reset process, following a power-up, front panel reset, or equivalent. Press the F2 key when prompted to enter Setup.

Note: The "Press F2 to enter Setup" prompt may be suppressed (see *Boot Options Sub-Menu, SETUP Prompt*) , but the F2 key still invokes the BIOS Setup program during system reset.

BIOS Configuration

BIOS setup is accomplished by making selections from a series of menus, shown in Figure 3-1.

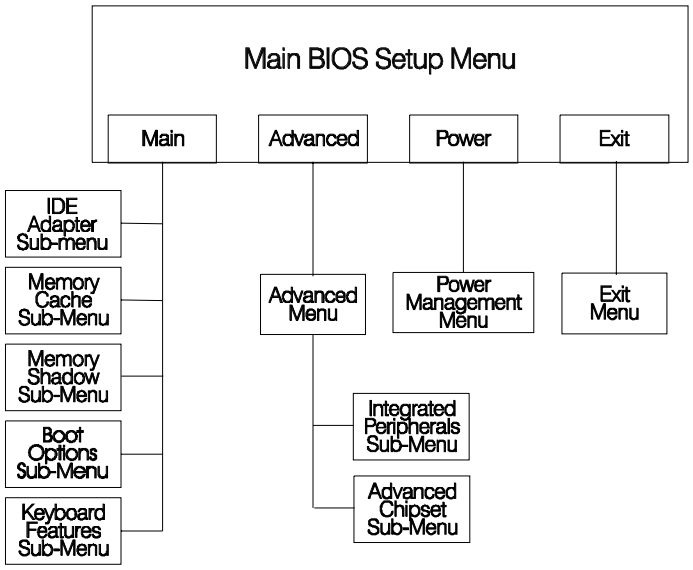


Figure 3-1. BIOS Setup Screen Menu Map.

Access to the setup screen is possible only during a short time during bootup when a message is displayed indicating that the "F2" key may be pressed to enter setup. This provides consistency of operation across all supported operating systems, and forces a direct correspondence between the displayed System BIOS setup settings and the hardware.

The up and down cursor (arrow) keys to move from field to field while the right and left arrows move from menu to menu, as noted in the menu bar at the top of each setup screen. If the arrow keys are used to leave a menu and then return, the active field is always at the beginning of the menu.

Fields with a triangle to the left are sub-menu headings. Press Enter when the cursor rests on one of these headings to reach that sub-menu.

Most fields consist of a series of selectable choices. Position the cursor at the field and use the + and - keys on the numeric keypad to rotate through the available choices. Once the desired entry appears, use the up and down arrow to move to the next field.

The fields in each menu and sub-menu are explained below the menu. Additional help information is available in the help area on the Setup screen.

Main Setup Menu

The Main Setup Menu is shown below:

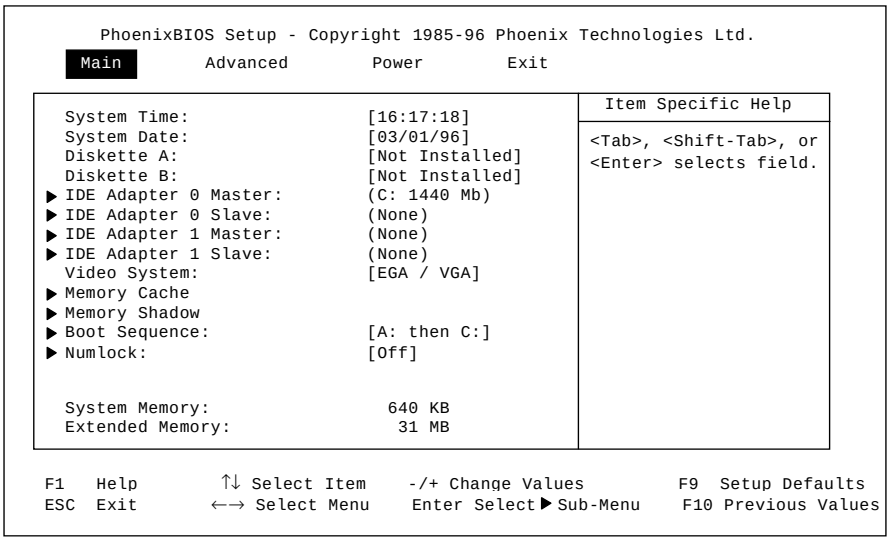

PhoenixBIOS Setup - Copyright 1985-96 Phoenix Technologies Ltd.
Main
Advanced
Power
Exit
System Time: [16:17:18]
System Date: [03/01/96]
Diskette A: [Not Installed]
Diskette B: [Not Installed]
▶ IDE Adapter 0 Master: (C: 1440 Mb)
▶ IDE Adapter 0 Slave: (None)
▶ IDE Adapter 1 Master: (None)
▶ IDE Adapter 1 Slave: (None)
Video System: [EGA / VGA]
▶ Memory Cache
▶ Memory Shadow
▶ Boot Sequence: [A: then C:]
▶ Numlock: [Off]
System Memory: 640 KB
Extended Memory: 31 MB
Item Specific Help
<Tab>, <Shift-Tab>, or <Enter> selects field.
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select ▶ Sub-Menu F10 Previous Values

Figure 3-2. Main BIOS Setup Menu

System Time:/System Date:

These values are changed by moving to each field and typing in the desired entry. The TAB key moves from hours to minutes to seconds, or from months to days to years.

Diskette A:/Diskette B:

This field identifies the type of floppy disk drive installed as the A:/B: drive. Possible settings are “Not Installed”, “360 KB, 5¼””, “720 KB, 3½””, “1.2 MB, 5¼””, “1.44 MB, 3½””, and “2.88 MB, 3½””. The BIOS defaults to “Not Installed” for drive A: and B:.

IDE Adapter 0/1 Master/Slave: Sub-menus

These fields are headings for menus that allow entering complete disk drive information. Once the information is entered for the drive, the entry in the Main Menu shows the drive selected. See “IDE Adapter Sub-menu” on page 3-5 for more information.

Video System:

This field is used to select the video type. Possible selections are: “EGA/VGA”, “CGA 80x25”, and “Monochrome”. The default is “EGA/VGA”.

Memory Cache Sub-menu

The term “Memory Cache” refers to the technique of caching BIOS images. See “Memory Cache Sub-menu” on page 3-20 for more information.

Memory Shadow Sub-menu

The term “Memory Shadow” refers to the technique of copying information from an extension ROM into DRAM and accessing it in this alternate memory location. See “Memory Shadow Sub-menu” on page 3-22 for more information.

Boot Sequence Sub-menu

The Boot Sequence Sub-menu allows changing the boot delay, boot sequence, and disabling several displays during the boot process, such as the SETUP prompt, POST errors, floppy drive check, and summary screen. Once the boot sequence has been set, it displays in this entry in the Main menu.

Keyboard Features (Numlock) Sub-menu

This menu enables or disables various keyboard features, including enabling the Numlock key, enabling the key click, and setting the keyboard auto-repeat rate and delay. The Numlock setting displays for this entry in the Main Menu.

System Memory

This field is not editable and displays the amount of conventional memory (below 1MB). No user interaction is required.

Extended Memory

This field is not editable and displays the amount of extended memory (above 1MB). No user interaction is required.

IDE Adapter Sub-menu

There are a total of four IDE adapter sub-menus for the primary and secondary hard disk controllers, each having a master and slave drive screen. The detailed characteristics of the drive connected to the adapter are available in the IDE Adapter 0 sub-menu, which displays the following screen:

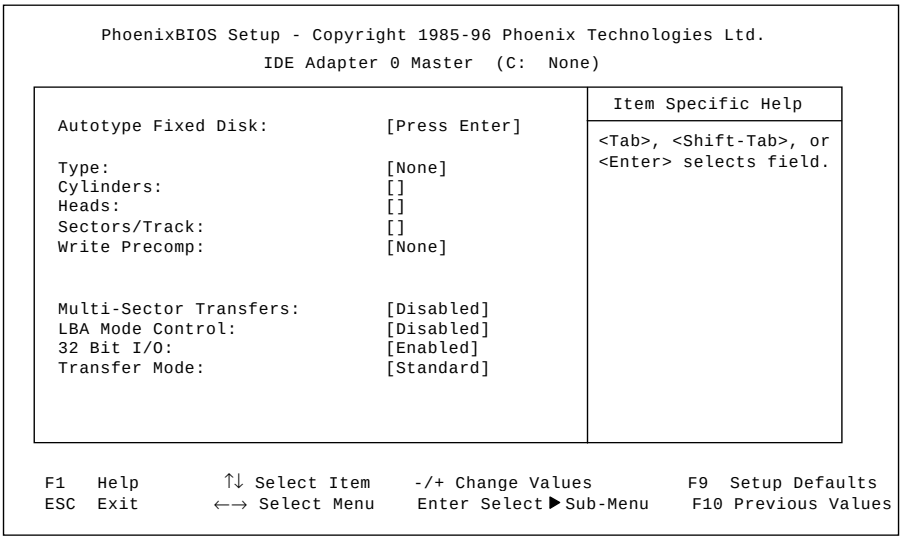

PhoenixBIOS Setup - Copyright 1985-96 Phoenix Technologies Ltd.
IDE Adapter 0 Master (C: None)
Item Specific Help
<Tab>, <Shift-Tab>, or <Enter> selects field.
Autotype Fixed Disk: [Press Enter]
Type: [None]
Cylinders: []
Heads: []
Sectors/Track: []
Write Precomp: [None]
Multi-Sector Transfers: [Disabled]
LBA Mode Control: [Disabled]
32 Bit I/O: [Enabled]
Transfer Mode: [Standard]
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select ▶ Sub-Menu F10 Previous Values

Figure 3-3. IDE Adapter Sub-Menu.

This option is used when setting up new disks and allows the Setup to determine the proper settings of the disk based on information on the disk, which is detected by Setup for drives that comply with ANSI specifications. The ENTER key is used to invoke this function.

Existing (formatted) disks must be set up using the same parameters that were used originally when the disk was formatted. The specific cylinder, head, sector information as listed on the label attached to the drive at the factory must be manually entered on this screen using a “User” type described below.

Type

"None" is selected if there is no IDE hard disk drive for this adapter. In the case for which there is an IDE disk but the "Autotype" feature cannot be employed, then the "User" type is selected and the correct drive values for cylinders, heads, sectors/track, and write precompensation for the drive are entered. Selecting "Auto" for this option causes the System BIOS to automatically autotype the hard disk every time POST is executed. The default is "Auto".

Multi-Sector Transfers

This option allows the user to configure the System BIOS to read ahead by the specified number of sectors whenever a disk access is performed. This has the effect of reading more data at once to reduce the absolute number of discrete disk reads performed by the operating system, which may increase system performance. The possible selections are "Disabled", "2 sectors", "4 sectors", "8 sectors", or "16 sectors" . Note that autotyping may change this value if the hard disk reports that it supports block accesses. The default is "Disabled".

LBA Mode Control

When enabled, this option allows the System BIOS to reference hard disk data as logical blocks instead of using the traditional Cylinders/Heads/Sectors (CHS) method. This option can only be used if both the hard disk being configured and the operating system support Logical Block Addressing (LBA). If disabled, then CHS mode is used. Note that autotyping may change this value if the hard disk reports that it supports LBA. The default is "Disabled".

32-bit I/O

This option allows the System BIOS to access the hard disk controller with 32-bit I/O accesses, increasing system performance. This selection is not affected by autotyping. If the PCI IDE controller in the T2 chipset is being used, then this option should be set to "Enabled" to maximize system performance. The default is "Enabled".

Transfer Mode

This option selects the mode that the System BIOS uses to access the hard disk. The selections are:

Standard (default)

Fast PIO 1

Fast PIO 2

Fast PIO 3

Fast PIO 4

Fast DMA A

Fast DMA B

Fast DMA F

Older hard disks only support “Standard”. Newer hard disks adhering to “Fast ATA” or “Enhanced IDE” specifications may support the fast programmed I/O or DMA modes. Note that autotyping may change this value depending on the transfer modes that the hard disk reports it supports. The fast DMA modes take full advantage of the onboard bus mastering hard disk controller and should yield the highest performance when used in conjunction with multitasking operating systems that support it. The default is “Standard”.

Boot Options Sub-menu

The Boot Options Sub-menu allows changing the boot sequence options. The Boot Options Sub-menu shown in Figure 3-4. Boot Options Sub-menu.displays:

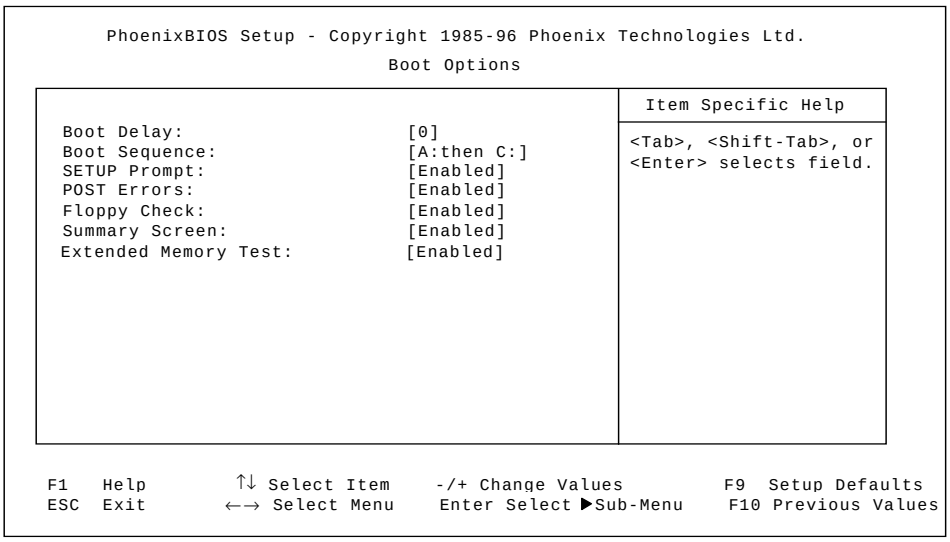

PhoenixBIOS Setup - Copyright 1985-96 Phoenix Technologies Ltd.
Boot Options
Item Specific Help
Boot Delay: [0]
Boot Sequence: [A:then C:]
SETUP Prompt: [Enabled]
POST Errors: [Enabled]
Floppy Check: [Enabled]
Summary Screen: [Enabled]
Extended Memory Test: [Enabled]
<Tab>, <Shift-Tab>, or <Enter> selects field.
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select ▶Sub-Menu F10 Previous Values

Figure 3-4. Boot Options Sub-menu.

Boot Delay:

This option is used to set the system to delay booting for a time period in seconds. This allows for long start up times on older boot devices that spin up slowly and ranges from 0 through 255 seconds. The default is “0” seconds.

Boot Sequence:

This option is used to define how the system treats floppy drive A: when booting. Booting can occur from a floppy in the A: drive or directly from the fixed disk drive. To reduce the amount of time required to boot, the boot sequence should be set to “C: only”. Note that the C: drive may be either an IDE or SCSI drive.

The options are as follows:

A: then C:	Used to boot from the floppy drive, or if no floppy disk is present in the A: drive, boot from the C: drive.
C: then A:	Used to boot from the C: drive, or if none is present, boot from the A: drive.
C: only:	Used to boot from the C: drive without searching for an A: drive.

The default is "A: then C:". The setting chosen here displays in the Boot Sequence Sub-menu prompt.

Setup Prompt:

This option is used to enable or disable the message "Press F2 to enter Setup." Even if the message is disabled, the F2 key can still be pressed at the appropriate time to enter the Setup Menu. The default is "Enabled".

POST Errors:

This option is used to stop during the boot process if the POST encounters errors. Otherwise, the system continues to attempt to boot despite any startup error messages that display. Note that this option only affects those errors defined in the section on Boot Failures in *Appendix D*. The default is "Enabled".

Floppy Check:

This option is used to enable or disable the floppy drive search during the boot. To speed up the boot process, the floppy check should be disabled. It is still possible to boot from the A: drive even with the floppy check disabled. The default is "Enabled".

Summary Screen:

This option is used to enable or disable a summary of the system configuration, which displays before the operating system starts to load. To speed up the boot process, the summary screen should be disabled. The default is "Enabled".

Extended Memory Test:

This option enables or disables testing of memory above 1MB during boot-up. To speed up the boot process, disable the extended memory test. The default is “Enabled”.

Keyboard Features Menu

Use this sub-menu to enable or disable various keyboard features.

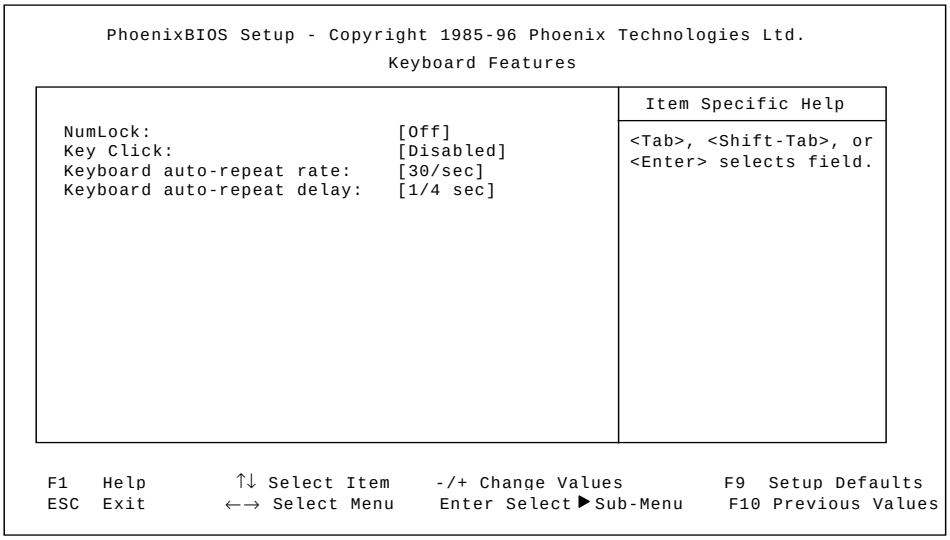

PhoenixBIOS Setup - Copyright 1985-96 Phoenix Technologies Ltd.
Keyboard Features
Item Specific Help
NumLock: [Off]
Key Click: [Disabled]
Keyboard auto-repeat rate: [30/sec]
Keyboard auto-repeat delay: [1/4 sec]
<Tab>, <Shift-Tab>, or <Enter> selects field.
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select ▶ Sub-Menu F10 Previous Values

Figure 3-5. Keyboard Features Sub-menu.

Numlock

This option is used to enable or disable the Numlock feature of the keyboard on booting. This enables the use of the keypad numbers. The default is “Off”, which automatically disengages the Numlock key at boot time.

Key Click:

This option is used to enable or disable the key click feature on the keyboard. If enabled, the system produces an audible click each time a key is pressed. The default is “Disabled”.

Keyboard auto-repeat rate:

This option is used to set the auto-repeat rate if holding a key down on the keyboard. The rates can be set to one of: “2/sec”, “6/sec”, “10/sec”, “13.3/sec”, “18.5/sec”, “21.8/sec”, 26.7/sec”, and “30/sec”. The default rate is “30/sec”.

Keyboard auto-repeat delay:

This option is used to set the delay between when a key is pressed and when the auto-repeat feature begins. Options are “1/4 sec”, “1/2 sec”, “3/4 sec”, and “1 sec” . The default delay is “1/4 sec”.

Advanced Menu

The Advanced Menu contains settings for integrated peripherals, memory shadow, cache, and large disk access mode.

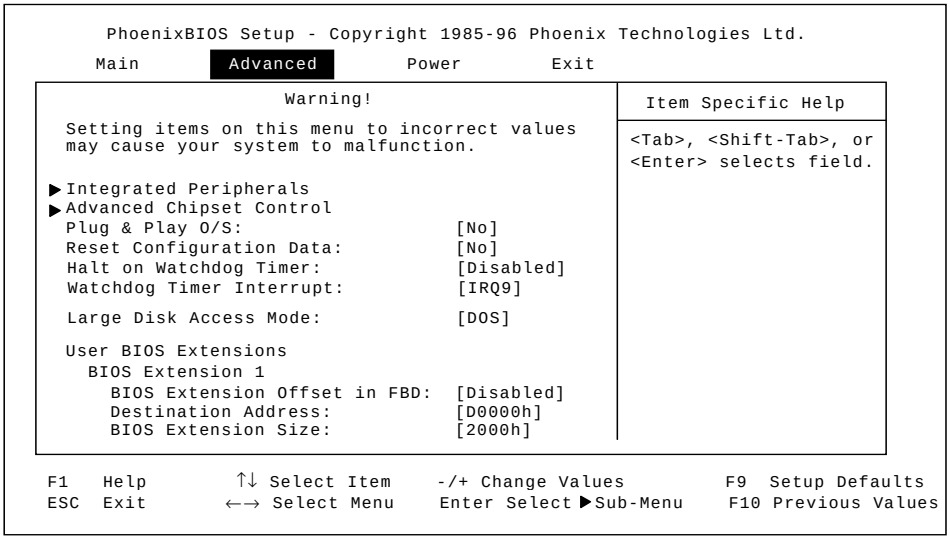

PhoenixBIOS Setup - Copyright 1985-96 Phoenix Technologies Ltd.
Main
Advanced
Power
Exit
Warning!
Setting items on this menu to incorrect values may cause your system to malfunction.
Item Specific Help
<Tab>, <Shift-Tab>, or <Enter> selects field.
▶Integrated Peripherals
▶Advanced Chipset Control
Plug & Play O/S: [No]
Reset Configuration Data: [No]
Halt on Watchdog Timer: [Disabled]
Watchdog Timer Interrupt: [IRQ9]
Large Disk Access Mode: [DOS]
User BIOS Extensions
BIOS Extension 1
BIOS Extension Offset in FBD: [Disabled]
Destination Address: [D0000h]
BIOS Extension Size: [2000h]
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select ▶Sub-Menu F10 Previous Values

Figure 3-6. Advanced Menu.

Integrated Peripherals Sub-menu

This option is used to select the Integrated Peripherals sub-menu in order to configure the onboard I/O ports, IDE controller, and Ethernet controller.

Advanced Chipset Control Sub-menu

This option is used to select the Advanced Chipset Control sub-menu in order to configure the chipset.

Plug & Play OS

If enabled, this option informs the System BIOS that the operating system that is booted supports Plug and Play. This forces the Plug and Play portion of the System BIOS to only configure motherboard devices and those peripherals that are necessary for booting (display, hard disk, etc.). Thus the operating system must configure the other devices and peripherals. The default is “No”.

Reset Configuration Data

If enabled, this option clears the Extended System Configuration Data (ESCD) block residing in FBD main block #2. This is necessary the first time a system is turned on or if the ESCD becomes corrupted. The default is “No”. This option is automatically reset to “No” after the ESCD is cleared.

Halt on watchdog reset

If enabled, this option causes the System BIOS to halt the boot process if it detects that a watchdog timer reset occurred. The default is “Disabled”.

Watchdog Timer Interrupt

This option specifies how IRQ9 is used by the watchdog timer. The possible selections are “Auto” and “Watchdog Timer”. When set to “Auto”, IRQ9 is available for use by PCI devices. When set to “Watchdog Timer”, IRQ9 is reserved for use by the watchdog timer. The default is”Auto”.

Large Disk Access Mode:

If a hard disk larger than 528MB is being used, this selection should be set to “DOS” if running MS-DOS, or set to “Other” if using a different operating system. When set to “DOS”, this selection causes the System BIOS to perform cylinder/head translation if the drive is configured in Setup to have more than 1024 cylinders. This allows MS-DOS systems to use hard disks up to 8GB (1024C x 255H x 63S) in size without special drivers or LBA. The default is “DOS”.

User BIOS Extensions

These items control the loading (shadowing) of BIOS extensions contained in the FBD main block #3. Note that there are actually three groups of Setup items to control the shadowing of up to three BIOS extensions. The screen graphic only shows the first group.

BIOS Extension Offset in FBD:

This option selects the source address of the BIOS extension located in the FBD. The address is an offset from the base of the FBD. The offset range is between 4A000h through 5E000h in 8KB increments. The default is “Disabled”.

Destination Address:

This option selects the target address of the BIOS extension which can range from CC0000h through DFFFFh in 8KB increments. The default is “D0000h”.

BIOS Extension Size:

This option selects the number of bytes to copy from the FBD into shadow memory. BIOS extension sizes can be selected in 8KB increments from 2000h through 10000h. The default is “2000h”.

Integrated Peripherals Sub-menu

The options in this sub-menu are used to configure the onboard serial and parallel port and disk controllers.

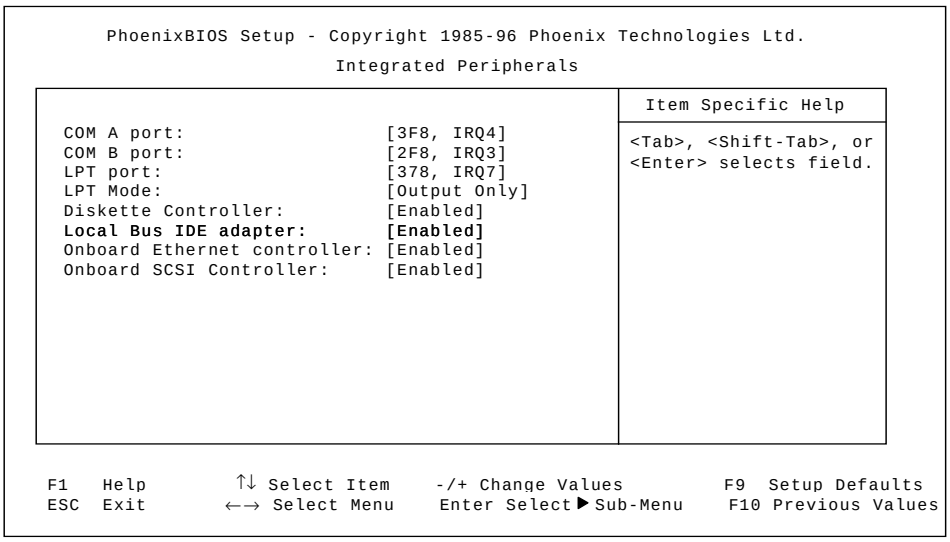

PhoenixBIOS Setup - Copyright 1985-96 Phoenix Technologies Ltd.
Integrated Peripherals
Item Specific Help
COM A port: [3F8, IRQ4]
COM B port: [2F8, IRQ3]
LPT port: [378, IRQ7]
LPT Mode: [Output Only]
Diskette Controller: [Enabled]
Local Bus IDE adapter: [Enabled]
Onboard Ethernet controller: [Enabled]
Onboard SCSI Controller: [Enabled]
<Tab>, <Shift-Tab>, or <Enter> selects field.
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select ▶ Sub-Menu F10 Previous Values

Figure 3-7. Integrated Peripherals Sub-menu.

COM A port

This option is used to configure the serial port labeled on the front panel as “COM A”. The choices for I/O base addresses and IRQs are: “Disabled”, “3F8, IRQ4”, “2F8, IRQ3”, “3E8, IRQ4”, “2E8, IRQ3”, and “Auto”. “Auto” causes the System BIOS to choose a base address and IRQ setting that avoids conflicting with the other ports. The default I/O base and IRQ for this COM port are “3F8, IRQ4”.

COM B port

This option is used to configure the serial port labeled on the front panel as “COM B”. The choices for I/O base addresses and IRQs are: “Disabled”, “3F8, IRQ4”, “2F8, IRQ3”, “3E8, IRQ4”, “2E8, IRQ3”, and “Auto”. “Auto” causes the System BIOS to choose a base address and IRQ setting that avoids conflicting with the other ports. The default I/O base and IRQ for this COM port are “2F8, IRQ3”.

LPT port

This option is used to configure the parallel port labeled on the front panel as “LPT”. The choices for I/O base addresses and IRQs are: “Disabled”, “378, IRQ7”, “278, IRQ5”, and “Auto”. “Auto” causes the System BIOS to choose a base address and IRQ setting that avoids conflicting with the other ports. The default I/O base and IRQ for this LPT port are “378, IRQ7”.

LPT Mode

This option sets the mode under which the bi-directional LPT port operates. The selections are:

Output only (the default)	Use this setting when the LPT port is used only to drive an output device, typically a printer.
Bi-directional	Allows bi-directional data flow on the LPT port, such as when a mass storage device shares the LPT port.

ECP

Diskette Controller

This option enables or disables the onboard floppy disk controller. The default is “Enabled”.

Local Bus IDE adapter

This option enables or disables the onboard PCIbus IDE hard disk controller channels. This option must be set to “Disabled” if a CompactPCI hard disk controller is installed in the system. The default is “Both”, which enables both the primary and secondary IDE channels.

Onboard Ethernet controller

This option enables or disables the onboard PCIbus Ethernet controller. The default is “Enabled”.

Onboard SCSI controller

This option enables or disables the onboard PCIbus SCSI controller. The default is “Enabled”.

Advanced Chipset Control Sub-menu

The options on this screen allow control over selected chipset settings that affect performance or function. The Advanced Chipset Control Sub-menu is shown below.

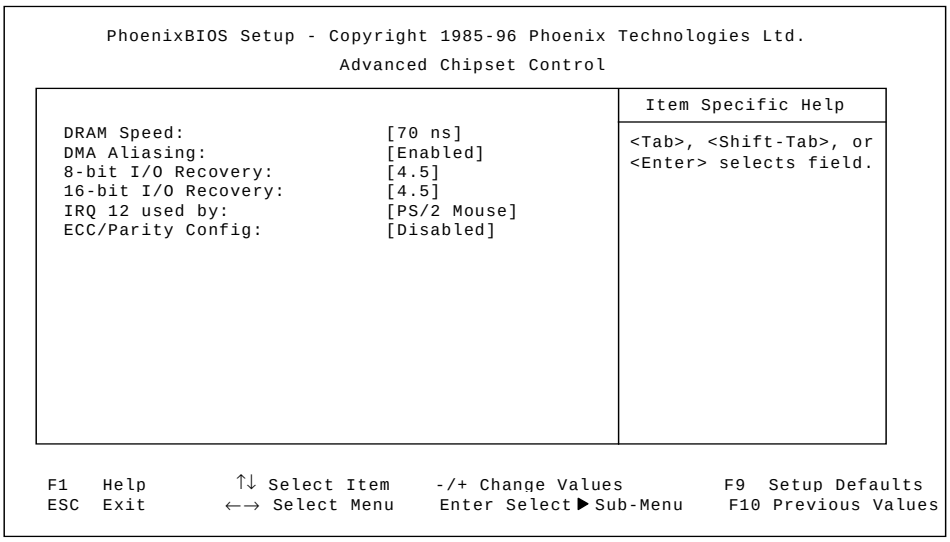

PhoenixBIOS Setup - Copyright 1985-96 Phoenix Technologies Ltd.
Advanced Chipset Control
Item Specific Help
DRAM Speed: [70 ns]
DMA Aliasing: [Enabled]
8-bit I/O Recovery: [4.5]
16-bit I/O Recovery: [4.5]
IRQ 12 used by: [PS/2 Mouse]
ECC/Parity Config: [Disabled]
<Tab>, <Shift-Tab>, or <Enter> selects field.
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select ▶ Sub-Menu F10 Previous Values

Figure 3-8. Advanced Chipset Control Sub-menu.

DRAM Speed

This option selects the speed of the installed DRAM SODIMMs. Selecting 70ns for 60ns SODIMMs decreases performance. Selecting 60ns for 70ns SODIMMs is invalid. The default is “70 ns”.

DMA Aliasing

This option allows I/O accesses to the range 90-9Fh (except 92h) to alias to 80-8Fh. If an ISAbus device uses the address range 90-9Fh, then this option must be disabled to access the device. The default is “Enabled”.

8-bit I/O Recovery

This option selects the number of ISAbus SYSCLKs to be inserted by the chipset between 8-bit back-to-back I/O accesses. Increasing the number of clocks decreases I/O performance but may allow slow devices to be accessed properly. This option can range from 3.5 through 11.5 SYSCLKs in 1 SYSCLK increments. The default is “4.5” SYSCLKs.

16-bit I/O Recovery

This option selects the number of ISAbus SYSCLKs to be inserted by the chipset between 16-bit back-to-back I/O accesses. Increasing the number of clocks decreases I/O performance but may allow slow devices to be accessed properly. This option can range from 3.5 through 7.5 SYSCLKs in 1 SYSCLK increments. The default is “4.5” SYSCLKs.

IRQ 12 used by

This option selects the routing of IRQ12. For systems without a PS/2 mouse, this option may be set to “PCI bus” to allow an ISAbus peripheral to use this interrupt line. Systems using a PS/2 mouse must have this option set to “PS/2 Mouse” for the mouse to operate correctly. Since the EPC-100 supports the PS/2 mouse connector, the default is “PS/2 Mouse”.

ECC/Parity Config

This option configures the DRAM controller to use no parity (“Disabled”), parity (“Parity”), or Error Checking and Correction (“ECC”) when accessing DRAM. Use of parity or ECC may improve system reliability since DRAM errors are likely to be detected by the chipset. Use of ECC allows for the detection of single and dual bit errors and the correction of single bit errors during DRAM reads. The parity and ECC selections require that all SODIMMs be x36 instead of x32. The “Disabled” selection can use either x32 or x36 SODIMMs. The default is “Disabled”.

Memory Cache Sub-menu

The options in this screen allow you to control whether or not certain memory regions are cached and whether or not the external Level 2 (L2) cache is enabled or disabled. The Memory Cache Sub-menu is shown below.

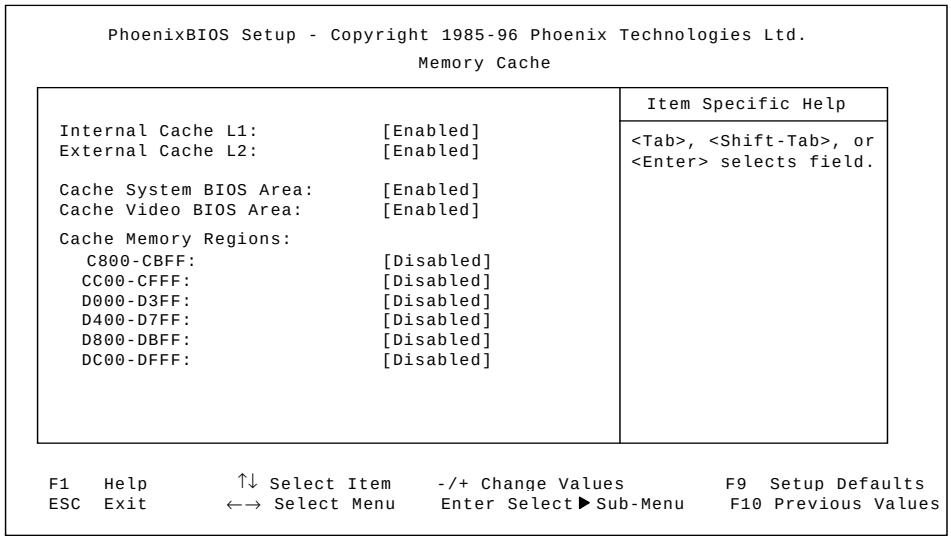

PhoenixBIOS Setup - Copyright 1985-96 Phoenix Technologies Ltd.
Memory Cache
Item Specific Help
<Tab>, <Shift-Tab>, or <Enter> selects field.
Internal Cache L1: [Enabled]
External Cache L2: [Enabled]
Cache System BIOS Area: [Enabled]
Cache Video BIOS Area: [Enabled]
Cache Memory Regions:
C800-CBFF: [Disabled]
CC00-CFFF: [Disabled]
D000-D3FF: [Disabled]
D400-D7FF: [Disabled]
D800-DBFF: [Disabled]
DC00-DFFF: [Disabled]
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select ▶ Sub-Menu F10 Previous Values

Figure 3-9. Memory Cache Sub-menu.

Internal Cache

This option enables or disables the Level 1 (L1) cache. The default is “Enabled”.

External Cache

This option enables or disables the Level 2 (L2) cache. The default is “Enabled”.

Cache System BIOS Area

This option enables or disables caching of the System BIOS area in the E0000h through FFFFFh DRAM area. The default is “Enabled”.

Cache Video BIOS Area

This option enables or disables caching of the VGA BIOS area in the C0000h through C7FFFh region. The default is “Enabled”.

Cache Memory Regions

These options enable or disable caching of the associated memory regions. When BIOS extensions are present in these regions, enabling caching for that region increases performance. The default is “Disabled”.

Memory Shadow Sub-menu

The term “shadowing” refers to the technique of copying BIOS extensions from ROM into DRAM and accessing them from DRAM. This allows the CPU to access the BIOS extensions much more quickly and generally increases system performance if many calls to the BIOS extensions are made. The Memory Shadow Sub-menu is shown below.

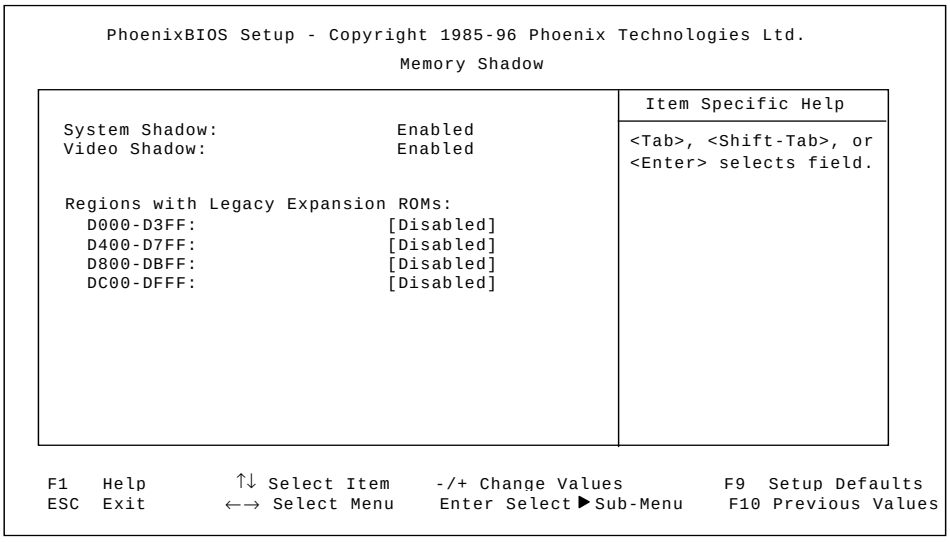

PhoenixBIOS Setup - Copyright 1985-96 Phoenix Technologies Ltd.
Memory Shadow
Item Specific Help
System Shadow: Enabled
Video Shadow: Enabled
<Tab>, <Shift-Tab>, or <Enter> selects field.
Regions with Legacy Expansion ROMs:
D000-D3FF: [Disabled]
D400-D7FF: [Disabled]
D800-DBFF: [Disabled]
DC00-DFFF: [Disabled]
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
ESC Exit ←→ Select Menu Enter Select ▶Sub-Menu F10 Previous Values

Figure 3-10. Memory Shadow Sub-menu.

The shadow regions should be used only if an CompactPCI card is installed in the system that contains a BIOS extension (ROM) although there is no effect on the system if a region is shadowed that does not contain a BIOS extension. Note that each shadow region in the setup menu is 16KB in size. Multiple shadow regions may have to be enabled if the BIOS extension to be shadowed is larger than 16KB.

System Shadow

This option is not editable since the System BIOS is always shadowed.

Video Shadow

This option is not editable since the VGA BIOS is always shadowed.

Shadow Memory Regions

These options enable or disable shadowing for the associated memory region. The default is “Disabled”.

Power Management Menu

The options in this menu provide control over the power management facilities. As the screen graphic below shows, only about one-half of the Power Management Menu Screen entries are visible at any one time; however, for completeness, all of the Power Management Menu entries are listed and annotated below.

System BIOS Power Management supported states are: Fully On, Standby Mode (partial power reduction), and Suspend Mode (maximum power reduction).

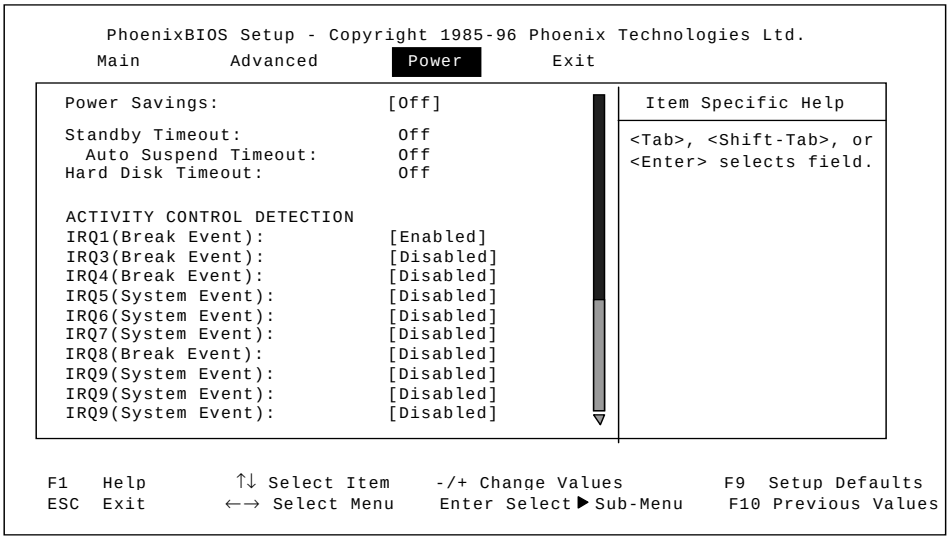


Figure 3-11. Advanced Power Management Sub-menu.

Power Savings

This option enables and selects the kind of power management, or it disables power management. The options are: “Off”, “Customize”, “Maximum Performance”, and “Maximum Power Savings. The default is “Off”.

Standby Timeout

This option enables and sets the inactivity duration required to elapse before the system is placed into Standby Mode, or it disables the Standby Timeout. The options are: “Off”, “2 min”, “15 min”, “30 min”, “1 hour”, “2 hours”, “3 hours”, and “4 hours”. The default is “Off”.

Auto Suspend Timeout

This option enables and sets the inactivity duration required to elapse before the system is placed into Suspend Mode from Standby Mode, or it disables the Suspend Timeout. The options are the same as for the Standby Timeout, enumerated above. The default is “Off”.

Hard Disk Timeout

This option specifies the duration of fixed disk access inactivity required to elapse before the system shuts off the disk drive, or it disables the Hard Disk Timeout. The options are: “Off”, “1 min”, “2 min”, “3 min”, “4 min”, “5 min”, “10 min”, and “16 min”. The default is “Off”.

Activity Detection Control

This option enables or disables a System or Break Event for the specified IRQ. A Break Event allows the system to run at full speed for the duration of the specified IRQ. Note that no such events are associated with IRQ0 and IRQ2, which are used by the PIIX3 bridge chip as system timer and cascade input interrupts, respectively.

IRQ1 (Break Event, Keyboard Controller)

This option enables or disables the Break Event for IRQ1. The options are: “Disabled” and “Enabled”. The default is “Enabled”.

IRQ3 (Break Event, COM B)

This option enables or disables the Break Event for IRQ3. The options are: “Disabled” and “Enabled”. The default is “Disabled”.

IRQ4 (Break Event, COM A)

This option enables or disables the Break Event for IRQ4. The options are: “Disabled” and “Enabled”. The default is “Disabled”.

IRQ5 (System Event, unused)

This option enables or disables the System Event for IRQ5. The options are: “Disabled” and “Enabled”. The default is “Disabled”.

IRQ6 (System Event, Floppy Disk Drive)

This option enables or disables the System Event for IRQ6. The options are: “Disabled” and “Enabled”. The default is “Disabled”.

IRQ7 (System Event, LPT1)

This option enables or disables the System Event for IRQ7. The options are: “Disabled” and “Enabled”. The default is “Disabled”.

IRQ8 (Break Event, Real-time Clock)

This option enables or disables the Break Event for IRQ8. The options are: “Disabled” and “Enabled”. The default is “Disabled”.

IRQ9 (System Event, Watchdog Timer)

This option enables or disables the System Event for IRQ9. The options are: “Disabled” and “Enabled”. The default is “Disabled”.

IRQ10 (System Event, unused)

This option enables or disables the System Event for IRQ10. The options are: “Disabled” and “Enabled”. The default is “Disabled”.

IRQ11 (System Event, unused)

This option enables or disables the System Event for IRQ11. The options are: “Disabled” and “Enabled”. The default is “Disabled”.

IRQ12 (Break Event, Mouse Controller)

This option enables or disables the Break Event for IRQ12. The options are: “Disabled” and “Enabled”. The default is “Disabled”.

IRQ13 (System Event, Numeric Coprocessor)

This option enables or disables the System Event for IRQ13. The options are: “Disabled” and “Enabled”. The default is “Disabled”.

IRQ14 (System Event, Primary IDE Controller)

This option enables or disables the System Event for IRQ14. The options are: “Disabled” and “Enabled”. The default is “Disabled”.

IRQ15 (System Event, unused or MIRQ for Secondary IDE Controller)

This option enables or disables the System Event for IRQ15. The options are: “Disabled” and “Enabled”. The default is “Disabled”.

SMI (System Event, Power Management or Watchdog Timer Event)

This option enables or disables the System Event for SMI. The options are: “Disabled” and “Enabled”. The default is “Disabled”.

NMI (System Event, PIIX3 Bridge when SERR# or IOCHK# is asserted by software)

This option enables or disables the System Event for NMI. The options are: “Disabled” and “Enabled”. The default is “Disabled”.

Exit Menu

The options in this menu allow saving settings and exiting, or abandoning changes and exiting to the system, or controlling the backup and restoration of CMOS RAM to the FBD.

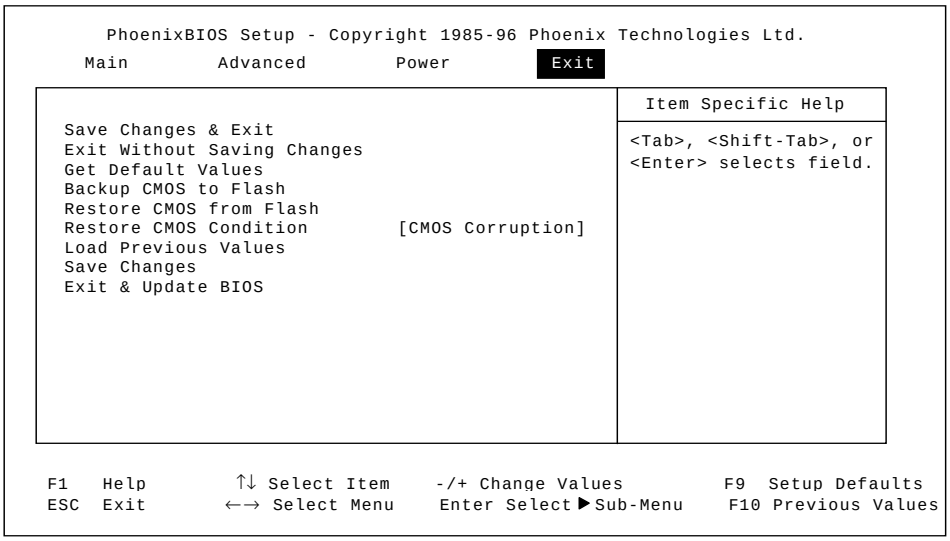


Figure 3-12. Exit Menu.

Save Changes & Exit

This option is used to save into CMOS the values that have been entered and reboots.

Exit Without Saving Changes

This option is used to discard the changes just made and revert to the state when Setup was entered. The system reboots with the old values.

Get default values

This option is used to reset the Setup values to the original, default values that were set at the factory, before any suppliers or other end users made changes.

BIOS Configuration

Backup CMOS to Flash

This option is used to immediately save current Setup settings to CMOS RAM and into FBD main block #1.

Restore CMOS from Flash

This option is used to immediately restore CMOS RAM and update current Setup settings from FBD main block #1.

Restore CMOS Condition

This option is used to determine under what conditions the System BIOS restores CMOS RAM from FBD main block #1 when booting. The restore conditions are: “Always”, “Never”, and “CMOS Corruption”. The default is “CMOS Corruption”.

Load previous values

This option is used to load the system with the previous values before an editing session started.

Save Changes

This option is used to save the edits made during a session.

Exit & Update BIOS

This option is used to initiate a System BIOS update.

Chapter 4 - Theory of Operation

Introduction

The EPC-100 is a double-slot 6U size module designed to the cPCI Revision 1.0 specification. It consists of a main board with the following connectors:

On the front panel:

- PS/2 style Keyboard Connector
- PS/2 style Mouse Connector
- Dual USB Connector
- 50-pin SCSI-II Connector
- 2 9-pin Serial Connectors
- DB-25 BiDirectional Parallel Port
- DB-15 SVGA Video Connector
- BNC and RJ45 Base 10/100 Ethernet Connectors

And on the rear panel:

- J1 cPCI Connector
- J2 cPCI Connector

The 100-200MHz Pentium Processor Module Daughter Board contains the following core functionality:

100-200 MHz Pentium Processor

256 or 512 KB of L2 Cache

Intel TXC System Controller

up to 256 MB of SODIMM DRAM

EIDE Controller consisting of two master and two slave drive controllers

System BIOS implemented as a Flash ROM supporting BIOS extensions

Block Diagram

Figure 4-1 shows the division and interconnection of EPC-100 functions. These are described below.

Processor Module Daughterboard

An Intel Pentium processor (with integral FPU) runs at 100, 133, 166, or 200 MHz. The processor, the TXC system controller, and the L2 cache all operate on a 60/66MHz local bus. The PCIbus runs at half the local bus speed (30/33MHz) and the ISA bus runs at one quarter the PCI bus speed (7.5/8.25 MHz).

Cache Memory

A second-level (L2) write-back 256 or 512KB main-memory cache is implemented by the Intel 82430HX chipset's TXC system controller.

Main System Memory

Main memory is implemented as SODIMM 72-pin socketed 3.3 volt DRAM. The main memory controller supports up to 256MB of 60 or 70 ns Fast Page Mode or EDO DRAM in two dual 72-pin SODIMM sockets. The CPU memory bus is 64 bits wide, so the SODIMM sockets must be populated with identical pairs of 32 bit DRAM modules. The TXC controller generates all of the required control signals, such as RAS#, CAS#, and WE#, as well as the multiplexed addresses for the DRAM array.

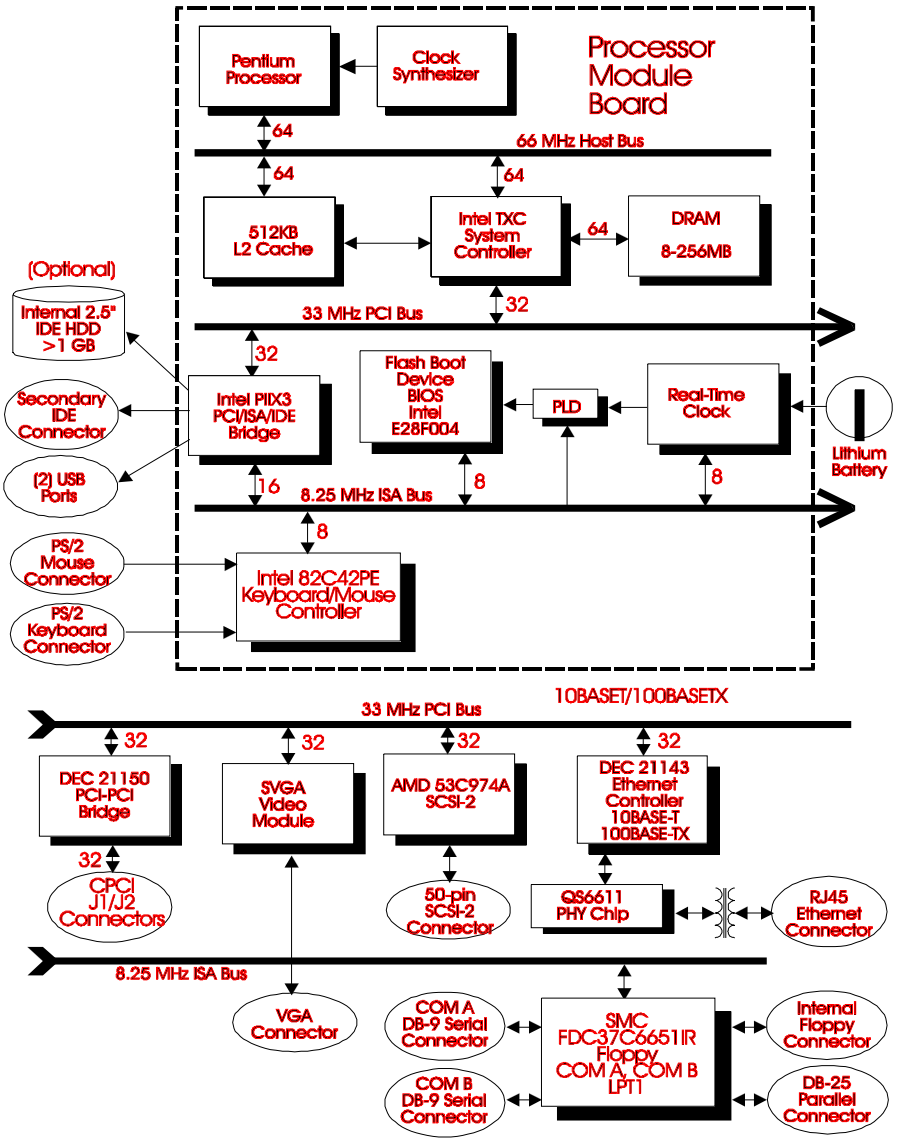


Figure 4-1. Block Diagram of the EPC-100.

Upgrading Main System Memory

At the time of writing, the the following sizes of 60 or 70ns Fast Page Mode or EDO DRAM were useable:

Type	Row/Column	Total Size (MB)	Number of SODIMMs
512Kx32	10/9	4	2
1Mx32	10/9 or 10/10	8	2
2Mx32	10/10 or 10/11	16	2
4Mx32	11/10, 11/11, or12/10	32	2
4Mx32	11/10, 11/11, or12/10	64	4
8Mx32	12/11	128	4
16Mx32	12/12	256	4

Table 4-1. Memory Upgrade DRAMs.

Memory Map

The 2^{32} byte physical address space seen by the Intel Pentium occupies three areas:

1. The area between 0 and 1 MB is largely defined by the IBM PC/AT architecture.
2. The area between 1 MB and 256 MB depends on how much DRAM is installed in the EPC-100.

Memory addresses from the Pentium or Pentium Pro between 0 and 4 MB (0FFFFFFFh) is mapped as follows:

Range	Content	Cacheable
00000000 - 0009FFFF	First 640 KB of DRAM (DOS memory)	yes
000A0000 - 000BFFFF	VGA video DRAM, mapped to the Video Module	no
000C0000 - 000C7FFF	Write-protected DRAM containing shadowed video BIOS	yes
000C8000 - 000CFFFF	SCSI BIOS extension	yes
000D0000 - 000DFFFF	BIOS Extensions	yes
000E0000 - 000FFFFF	System BIOS Shadow	yes
10000000 - FFF7FFFF	ISA Bus (aliased)	no
FFF80000 - FFFFFFFF	BIOS	no

Table 4-2. System Memory Map.

Interrupt Usage

The EPC-100 PC-compatible interrupt usage is as follows:

Interrupt	**Interrupt Function**
IRQ0	System timer (internal PIIX3 connection)
IRQ1	Keyboard controller
IRQ2	Cascade interrupt input (internal PIIX3 connection)
IRQ3	COM B (if enabled)
IRQ4	COM A (if enabled)
IRQ5	unused
IRQ6	Floppy (if enabled)
IRQ7	LPT1 (if enabled)
IRQ8	Real time clock
IRQ9	Watchdog (if enabled)

(cont'd)

Interrupt	Interrupt Function
IRQ10	unused
IRQ11	unused
IRQ12	Mouse
IRQ13	Numeric coprocessor FERR# (internal PIIX3 connection)
IRQ14	Primary IDE
IRQ15	unused (MIRQ0 for secondary IDE)
NMI	PIIX3 when SERR# or IOCHK# is asserted (software controlled)
SMI	Power management / Watchdog Timer Event.
PIRQA	CompactPCI Bus
PIRQB	Ethernet & CompactPCI Bus
PIRQC	SCSI & CompactPCI Bus
PIRQD	USB & CompactPCI Bus

Note that PIRQ[A-D] correspond directly to the PCI interrupts INT[A-D]. The software may steer these interrupts to any of the 11 interrupts (IRQ[15,14, 12-9, 7-3]) using the MBIRQx Route Control Register. Note also that the secondary IDE channel is assigned to MIRQ0 by the PIIX3 (when not using the APIC, as on EPC-100).

Table 4-3. Interrupt Usage.

Watchdog Timer

The watchdog timer is a binary counter which, upon overflow, will signal a watchdog timer event. The counter will cause a watchdog event after 128 ms, 1.02 second or 8.2 seconds (depending on the value of WDTV, bits 0 and 1 in register 8150h) if the application software does not reset the timer by writing to I/O location 8150h before the set time passes. An I/O write to address 8150h resets the counter.

If WDTV (bits 1 and 0 of register 8150h) are nonzero, the following occurs in response to a time-out event: The watchdog event register is set. If WDIE (bit 2 of register 8150h) is zero, IRQ9 is taken high to signal a watchdog time-out via interrupt. If WDIE (bit 2 of register 8150h) is set, a local “warm” hardware reset occurs. This reset clears the WDIE bit removing the reset condition. When exiting a hardware reset condition, the BIOS can check the WDEV bit. If this bit is set, then a

watchdog time-out caused the hardware reset (as opposed to SYSRESET or power-on reset). Depending on the value of a setup option the BIOS will then either HALT the CPU or allow the boot process to continue.

Service of a watchdog interrupt is signaled to the counter by writing the register at I/O 8150h. This will reset the counter and reset the signal driving IRQ9.

Flash Boot Device

The Intel E28F004BX-T is used as a Flash Boot Device (FBD). This is flash-updatable BIOS containing the boot, main, and parameter blocks shown in Figure 4-2 and shadowed at the top of 32-bit address space. The use of the FBD allows reprogramming of the main and parameter blocks of the BIOS.

The Plug-and-Play ESCD is also stored in the Boot-Block flash device in the block addressed from FFFA0000h-FFFBFFFFh. This block is always accessible for re-programming.

The boot block is NEVER reprogrammed by the user, even when the main and parameter blocks are reprogrammed. The capability to program the boot block is provided to facilitate changes by RadiSys manufacturing.

A “force recovery” jumper is provided that is connected to the P1-3 input of the 82C4PE keyboard controller. This jumper is readable by the boot block and can force the boot block to initiate a recovery sequence at power-up should other methods of initiating the sequence become inaccessible. (i.e. crisis recovery)

The system BIOS is shadowed in write protected DRAM at 000E0000h-000FFFFFh during system boot.

The flash BIOS device is memory addressed and resides in the last 512KB of system memory at address FFF80000h to FFFFFFFFh.

Keyboard/Mouse Controller

The Intel 82C42PE mouse/keyboard controller can interface to most standard PC mice and keyboards with PS/2-style connectors. The keyboard controller uses interrupt IRQ1 and the mouse uses IRQ12.

BIOS ROM and ROM Shadowing

The EPC-100 utilizes a Flash Boot Device (FBD) as its BIOS ROM. The BIOS ROM is mapped into the top of the processor's 32-bit address space. The BIOS consists of a 16 KByte boot block and the System BIOS in the 96KB Main block and both 8KB parameter blocks. The layout is described in Figure 4-2.

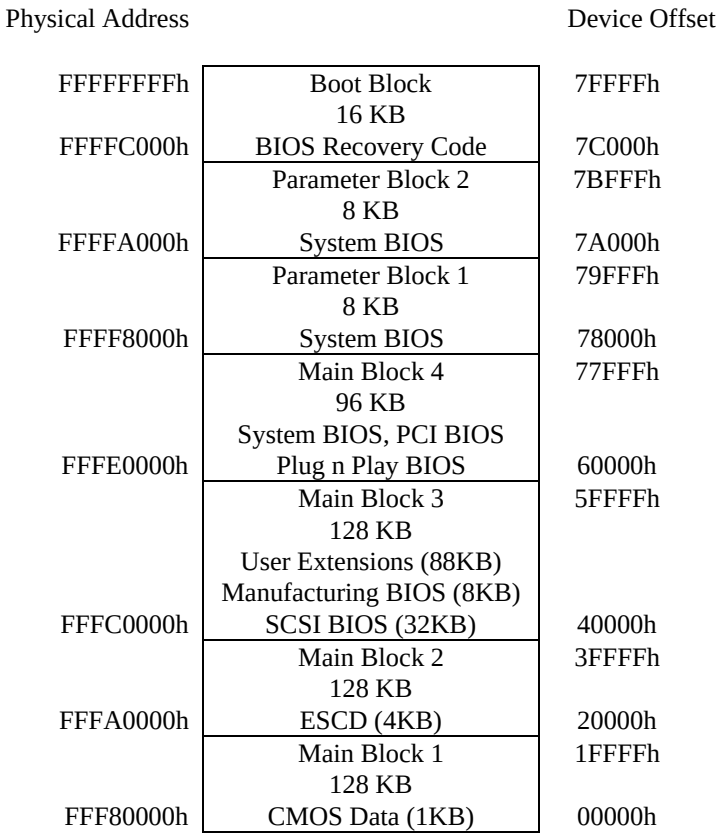


Figure 4-2. Flash Boot Device Memory

The BIOS initialization software copies the ROM contents into DRAM (a process called *shadowing*) at addresses E0000h-FFFFFh. The VGA BIOS is copied into C0000h-C7FFFh of DRAM. After copying into these areas, the BIOS write-protects them. Subsequent writes to these areas complete successfully but do not alter the data in DRAM.

There are two parameter blocks, each 8KB in size, used for BIOS code.

CMOS Save and Restore (CSR)

CMOS memory is backed up to and restored from Main Block 1 of the FBD as determined by the settings in the BIOS Setup Exit Menu. This allows you to save your settings to nonvolatile flash memory and to specify the conditions under which CMOS is to be restored from the FBD. For more information, see the Exit Menu section of *Chapter 3 - BIOS Configuration*.

Ethernet Controller

The EPC-100 implements 10/100BaseT Ethernet communications by using the DEC 21143-TA Ethernet Controller chip coupled to a QSI 6611 Physical Interface (PHY) chip that provides wave shaping and line filtering for both 10- and 100-Mbps operation, adaptive equalization, baseline wander compensation, 10/100 switching, and clock generation and recovery. The 21143 chip interfaces to the 32-bit PCI bus and the QS6611 provides the line driver and receiver for a 10BASE-T and 100BASE-TX Fast Ethernet connection to Category 5 unshielded twisted-pair cable via an RJ45 connector. 10BASE2 is supported through a BNC connector on the front panel.

This controller uses PCI INTB and REQ0/GNT0. It is configured through the PCI Configuration Space.

The Ethernet driver for Windows NT/4.0 is supplied by Digital Equipment Corporation and is supplied on a separate floppy diskette.

Product: DC21X4.SYS
Software revision: 4.15
Document release date: 1-6-97

Battery

The battery powers the CMOS RAM and TOD clock when system power is not present. At 60°C, the battery should have a shelf life of over four years. In a system that is powered on much of the time and where the ambient power-off temperature is less than 60°C, the battery is estimated to have a life of 10 years.

If system power is present, the +5V voltage also powers the CMOS RAM and TOD clock. This is done with the RTC chip's internal isolation diodes, so that either the onboard battery or the +5V power supply voltage can supply power and neither power source affects the other.

The 3.0V lithium battery supplied with the EPC-100 is a Renata CR2032 "coin cell" or equivalent. It is mounted on the main circuit board, beneath the EPC-100 Video Board. Should the battery fail, you may obtain and install a replacement.

Write down all of the CMOS setup parameters while the battery is still good, or save them, using the CMOS save and restore feature of the BIOS configuration Exit Menu.

To replace the battery:

1. Turn off the power and remove the EPC-100 from the cPCI chassis.

☞ **IMPORTANT: You should perform all of these steps in a static-free or ESD-protected environment.**

2. Remove the two jack screws securing the SVGA connector to the front panel.
3. Remove the five screws securing the I/O board (the narrow board with the serial and parallel port connectors) to the main board and the six jack screws securing the serial and parallel port connectors to the front panel.
4. Remove the I/O board.
5. Remove the two screws securing the video board to the main board.
6. Remove the video board.
7. Locate the battery, then slide the old battery out in the direction shown in Figure 4-3.
8. Slide the new battery into place, positive (+) side up
9. Reassemble the EPC-100.

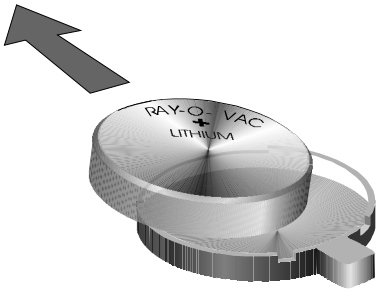


Figure 4-3. Replacing the Lithium CMOS Battery.

☞ **CAUTION: There is danger of explosion if battery is incorrectly replaced. Replace only with same or equivalent type recommended by RadiSys. Dispose of used batteries according to manufacturer's instructions.**

Peripheral Ports

The I/O address and IRQ of the peripheral ports are determined by the CMOS parameters established by default and modified via BIOS Setup screens. These include (2) RS-232 Serial Ports, a bidirectional parallel port, and (2) Universal Serial Bus (USB) ports. The RS-232 ports and the parallel ports, along with the floppy disk controller, are implemented by the SMC FDC37C665IR Super I/O Chip.

The address map for the Super I/O Chip is shown in Figure 4-4.

Address	Block Name	Notes
03F0-03F1h	Configuration	Write only[1,2]
03F0-03F1h	Floppy Disk	Read only[2]
03F2-03F5h, 03F7h	Floppy Disk	[2]
03F8-03FFh	Serial Port, COM1	[2]
02F8-02FFh	Serial Port, COM2	[2]
0278-027Ah	Parallel Port, LPT1	[2]
01F0-01F7h, 03F6h, 03F7h	IDE (not used)	AT Mode[2,3]

Table 4-4. Super I/O Chip Address Blocks.

Notes:

1 Configuration registers can only be modified by writing a security code sequence to 3F0h. The configuration registers can only be read in configuration mode by accessing 3F1h. Access to status registers A and B of the floppy disk is disabled in configuration mode. Outside of configuration mode, a read of 3F0h accesses status register A and a read of 3F1h accesses status register B of the floppy disk.

2 Default address. These addresses can be changed in configuration setup.

3 Addresses 320-323h and 3F5-3F7h for XT Mode. This is selected in configuration setup.

This Super I/O chip only decodes the I/O address space with the 10 LSBs. Additional circuitry gates the address enable with the upper six bits of the I/O address range (which must be all zero to allow AEN to pass.) The ECP registers located 778-77Ah are also decoded and allowed to pass to the Super I/O chip. Therefore, the address of the chip is decoded to 16 bits, with the top six expected to be zero.

RS-232 Ports

The RS-232 ports are standard PC COM serial ports based on the 16550 architecture. COM A is normally mapped to I/O address 3F8h-3FFh and uses interrupt IRQ4. If not needed, COM B can be disabled in the BIOS Setup Integrated Peripherals Sub-Menu to free up the I/O address and interrupt for usage by other expansion products. COM B is mapped to I/O address 2F8h-2FFh and uses interrupt IRQ3.

Parallel Port

The printer port is a bi-directional IEEE1284-C PC parallel port. The parallel port supports bi-directional communication compatible with the PS/2 definition. It is configured as LPT1 and mapped to I/O address 378h-37Fh and uses interrupt IRQ7. If not needed, LPT1 can be disabled in the BIOS Setup Integrated Peripherals Sub-Menu to free up the I/O address and interrupt for usage by other expansion products.

Floppy Controller

The SMC FC37C665IR Super I/O chip, used to implement the serial and parallel ports, is also used to implement a standard PC floppy disk port. The device resides on the ISA bus, and is accessed at the standard PC I/O addresses of 3F0h-3F7h. Interrupts are signaled on IRQ6.

The floppy interface connector is located on the I/O board and is not available at the front panel because it is normally only used for diagnostics or for initializing the hard disk(s).

USB Ports

The Universal Serial Bus (USB) controller is a host/hub controller and moves data between the main system memory and devices on the serial bus. The USB controller also includes the first level hub. This permits connection of two USB peripheral devices directly to the PIIX3 without an external hub. If more devices are required, an external hub can be connected to any one of the built in ports.

USB architecture has the concept of all devices connected to it being serviced through two software layers known as SBS (serial bus services) and HCS (host controller services). SBS allocates the necessary bandwidth for every device connected on the bus and builds a scheduler to service these devices at the required intervals. SBS passes the schedule information to the HCS layer. The HCS uses this information to build a schedule table and command blocks that hardware understands. The schedule table and command blocks are located in the system memory and contain information including the addresses for data movements to/from system memory. The current implementation of the USB support software may not support these features at initial product availability.

Two host-side USB ports are provided on the front panel. The USB root hub is built into the PIIX3 chip as part of the 82430HX chip set. The USB's PCI configuration

registers are located as function 2 of the PIIX3 configuration space and utilize PCI INTD.

Front Panel Indicators

6 LEDs on the front panel are used as system activity indicators:

RUN (green)	The RUN LED is lit whenever a write access to DRAM is made. This provides a normally lit LED indicating that the CPU is running. It is not lit if the CPU is halted or is executing entirely out of the on-chip cache.
cPCI (green)	The cPCI LED is lit whenever there is activity on the CompactPCI bus. The LED is tied to the FRAME# signal on the CompactPCI bus. This provides a normally lit LED indicating an access to resources on the CompactPCI bus
SCSI (green)	The SCSI LED is lit whenever the SCSI controller is active. This LED indicates the SCSI controller's chip select has been activated.
IDE (green)	The IDE LED is lit whenever a primary or secondary channel hard disk is accessed. This signal indicates a hard disk's chip select has been activated. It is asserted when an access to any of the hard drive addresses occurs.
ETHERNET (green)	The ETHERNET green LED indicates the Ethernet activity. The LED indicates the transmit or receive activity for the 10BASE–T, 100BASE–TX, or 10BASE2 network connections. When on, a packet is being transmitted or received. When off, there is no transmission activity.
ETHERNET (yellow)	The ETHERNET yellow LED indicates the Ethernet link status. When on, the adapter has a valid link on its network connection and is ready for normal operation (10BASE–T link or 100BASE–TX link). When off, the adapter did not find a valid 10/100BASE-TX link on its network connection; transmit and receive are not possible. Note that this LED is always off when using 10BASE2.

Chapter 5 -
Support and Service

In North America

Technical Support

RadiSys maintains a technical support phone that is staffed weekdays (except holidays) between 8:00 AM and 5:00 PM Pacific time. If you require assistance outside these hours, you can leave a message on voice-mail using the same phone number. You can also request help via electronic mail or by FAX addressed to RadiSys Technical Support Department. See the cover of this manual for the RadiSys telephone and FAX numbers. The RadiSys e-mail address on the Internet is ***support@radisys.com***. If you are sending e-mail or a FAX, please include information on both the hardware and software being used and a detailed description of the problem, specifically how the problem can be reproduced. We will respond by e-mail, phone or FAX by the next business day.

Technical support services are designed for customers who have purchased their products from RadiSys or an authorized sales representative. If your RadiSys product is part of a piece of OEM equipment, or was integrated by someone else as part of a system, support will be better provided by the OEM or system vendor that did the integration and understands the final product and environment.

World Wide Web

RadiSys maintains an active site on the World Wide Web. The home-page URL is *http://www.radisys.com*. The site contains current information about the company and locations of sales offices, new and existing products, contacts for sales, service, and technical support information. You can also send e-mail to RadiSys using the web site. Requests for sales, service, and technical support information receive prompt response.

Support and Service

Repair Services

RadiSys provides Factory Repair Service for the entire RadiSys product line. Standard service for all RadiSys products covers factory repair with customers paying shipping to the factory and RadiSys paying for return shipment. Overnight return shipment is available at customer expense. Normal turn-around time for repair and re-certification is five working days.

Quick Exchange services (immediate shipment of a loaner unit while the failed product is being repaired) are available. Negotiate these or other extra-cost services in advance to allow RadiSys to pool the correct product configurations. RadiSys does not maintain a general “loaner” pool: units are available only for customers who have negotiated this service in advance.

RadiSys does not provide a fixed-price “swap-out” repair service. Many customers indicate that issues of serial number tracking and version control make it more convenient to receive their original products back after repair.

Warranty Repairs

RadiSys will repair at no charge products having manufacturing defects during the warranty period. See the warranty information at the front of this manual. Products without fault sent in for warranty repair will be subject to a recertification charge. Extended warranties are available at a standard price for any product still under original warranty. RadiSys will gladly quote prices for extended warranties on products with lapsed original warranties; contact the factory if this applies.

Customer induced damage (resulting from misuse, abuse, or exceeding the product specifications) is not covered by warranty.

Non-Warranty Services

There are several classes of non-warranty service. These include repair of customer induced problems, repairs of failures for products outside the warranty period, recertification (functional testing) of a product either in or out of warranty, and procurement of spare parts.

All non-warranty repairs are subject to service charges. RadiSys has determined that pricing repairs based on time and materials is more cost-effective for the customer than a flat-rate repair charge. RadiSys analyzes the product after it is received. When instructed to do so, RadiSys informs the customer of repair costs for authorization. After the customer authorizes repairs and makes billing arrangements, RadiSys repairs the product and returns it to the customer.

Support and Service

RadiSys provides a recertification service for products either in or out of warranty. This service verifies correct operation of a product by inspecting and testing the product using standard manufacturing tests. There is a product-dependent charge for recertification.

Generally, very few components are field-repairable. However, since RadiSys understands that some customers want or need the option of repairing their own equipment, all components are available in a spares program. RadiSys charges a minimum billing for this program.

Arranging Service

To schedule service for a product, please call the RadiSys RMA Dispatcher. The telephone number appears on the cover of this manual. Have the product model and serial numbers available, along with a description of the problem. The RMA Dispatcher will issue a Returned Materials Authorization (RMA) number, a code number by which RadiSys tracks the product while it is being processed. Once you receive the RMA number, follow the instructions of the technical support representative and return the product to RadiSys, freight prepaid. Mark the RMA number clearly on the exterior of the package. If possible, re-use original shipping containers and packaging. In any case, be sure you follow good ESD-control practices when handling the product. Use anti-static bags and packing materials with adequate padding and shock-absorbing properties.

Before you ship the product, include the following information: return address, contact names and phone numbers in purchasing and engineering, and a description of the problem. If available, include ancillary information related to the problem.

Ship the product, freight prepaid, to the RadiSys Product Service Center at the address shown on the front cover of this manual.

Other Countries

Use the RadiSys web site to contact us, or contact the sales organization from which you purchased your RadiSys product for service and support.

Appendix A - Chipset and I/O Map

Introduction

This section contains the port I/O addresses for the address-mapped devices in the EPC-100. As is standard for the ISA bus, the A[15:0] bits are decoded for the 0200h-03FFh range and A[15] and A[9:0] are decoded for addresses above 8000h.

Table A-1. I/O Address Mapping for the EPC-100

First (8-bit) DMA controller		
I/O Addr	Functional group	Usage
000	DMA	Channel 0 address
001		Channel 0 count
002		Channel 1 address
003		Channel 1 count
004		Channel 2 address
005		Channel 2 count
006		Channel 3 address
007		Channel 3 count
008		Command/status
009		DMA request
00A		Command register (R)
		Single-bit DMA req mask(W)
00B		Mode
00C		Set byte pointer (R)
		Clear byte pointer (W)

First (8-bit) DMA controller (cont'd)		
I/O Addr	Functional group	Usage
00D		Temporary register (R)
		Master clear (W)
00E		Clear mode reg counter (R)
		Clear all DMA req mask(W)
00F		All DMA request mask
First Interrupt controller		
020	Interrupt controller 1	Port 0
021		Port 1
Counter-Timer functions		
040	Timer	Counter 0
041		Counter 1
042		Counter 2
043		Control (W)
Keyboard Port		
060	Keyboard controller	Data I/O register
061	NMI status	PIIX3
064	Keyboard controller	Command/status register - resets IRQ1 and 12/M

Time-of-Day Clock			
I/O Addr	Functional group	Usage	
070	Real-time clock	RTC index reg / NMI enable	
071		RTC data register (64 bits)	
		0	seconds
		1	seconds alarm
		2	minutes
		3	minutes alarm
		4	hours
		5	hours alarm
		6	day of week
		7	date of month
		8	month
		9	year
		A	status A
		B	status B
		C	status C
		D	status D
		E…3F	RAM
Phoenix NuBIOS			
080		Phoenix BIOS Status Information	

DMA Page Registers		
I/O Addr	Functional group	Usage
081	DMA	Channel 2 page register
082		Channel 3 page register
083		Channel 1 page register
087		Channel 0 page register
089		Channel 6 page register
08A		Channel 7 page register
08B		Channel 5 page register
08F		Refresh page register
Second Interrupt Controller		
0A0	Interrupt controller 2	Port 0
0A1		Port 1
Power Management Controller		
0B2	Power Management	Control
0B3		Status
DMA Controller		
0C0	DMA	Channel 4 address
0C2		Channel 4 count
0C4		Channel 5 address
0C6		Channel 5 count
0C8		Channel 6 address
0CA		Channel 6 count
0CC		Channel 7 address
0CE		Channel 7 count
0D0		Command/status
0D2		DMA request

DMA Controller (cont'd)		
I/O Addr	Functional group	Usage
0D4		Command register (R)
		Single-bit DMA req mask(W)
0D6		Mode
0D8		Set byte pointer (R)
		Clear byte pointer (W)
0DA		Temporary register (R)
		Master clear (W)
0DC		Clear mode reg counter (R)
		Clear all DMA req mask (W)
0DE		All DMA request mask
0E0		Phoenix BIOS Status Information
Coprocessor Interface		
0F0	Coprocessor	Clear coprocessor busy
0F1		Reset coprocessor
IDE Control		
170	Secondary IDE Control	Data Register
172		Sector Count
173		Sector Number
174		Cylinder LSB
175		Cylinder MSB
176		Drive/ Head
177		Status/ Command
1F0	Primary IDE Control	Data Register
1F2		Sector Count
1F3		Sector Number
1F4		Cylinder LSB
1F5		Cylinder MSB
1F6		Drive/ Head
1F7		Status/ Command

ISA Plug and Play		
I/O Addr	Functional group	Usage
279	Plug and Play	
A79		Data Register
CF8		Configuration Address Register
CF9		Turbo reset control register
CFC		Configuration data register
Serial I/O (COM B) Port		
2F8	COM B serial port	Receiver/transmitter buffer
		Baud rate divisor latch (LSB)
2F9		Interrupt enable register
		Baud rate divisor latch (MSB)
2FA		Interrupt ID register
2FB		Line control register
2FC		Modem control register
2FD		Line status register
2FE		Modem status register
Parallel I/O (LPT1) Port		
378	LPT1 parallel port	Printer data register
379		Printer status register
37A		Printer control register
EPP Registers		
37B	EPP	Address Port
37C		Data Port 0
37D		Data Port 1
37E		Data Port 2
37F		Data Port 3

VGA		
I/O Addr	Functional group	Usage
3B4	VGA	CRT Controller index
3B5		CRT Controller data
3BA		Feature control output, Input status
3C0		Attribute controller Index/Data
3C1		Attribute controller Index/Data
3C2		Miscellaneous output, Input status
3C3		Sleep
3C4		Sequencer Index
3C5		Sequencer Data
3C6		Video DAC pixel mask, Hidden DAC register
3C7		Pixel address read mode, DAC state
3C8		Pixel mask write mode
3C9		Pixel data
3CA		Feature control readback
3CC		Miscellaneous output readback
3CE		Graphics controller index
3CF		Graphics controller data
3D4		CRT controller index
3D5		CRT controller data
3DA		Feature control, pinput status
3F0		Configuration 37C651 Super I/O Combo chip
3F1		Configuration 37C651 Super I/O Combo chip
46E8	VGA	Adapter Sleep

Serial I/O (COM A) Port			
I/O Addr	Functional group	Usage	
3F8	COM A serial port	Receiver/transmitter buffer	
		Baud rate divisor latch (LSB)	
3F9		Interrupt enable register	
		Baud rate divisor latch (MSB)	
3FA		Interrupt ID register	
3FB		Line control register	
3FC		Modem control register	
3FD		Line status register	
3FE		Modem status register	
Interrupt Control Registers			
4D0	Interrupt	PIIX3 Edge/ level control - Int1	
4D1		PIIX3 Edge/ level control - Int2	
ECP Registers			
778	ECP	Data FIFO/ Config Register A	
779		Data FIFO/ Config Register B	
77A		Extended Control Register	
Watchdog Control and System Slot ID			
8150	Watchdog Control and System Slot ID	Bit	Usage
		0	WDTV - Watchdog Timer Value
		1	WDTV
		2	WDIE - Watchdog Timer Interrupt Event
		3	WDEV - Watchdog Event
		4	ENEV - ENUM# Event
		5	ENIE - ENUM# Interrupt Event
		6	Reserved
		7	Reserved

ENIE — ENUM# interrupt enable. If 1, the cPCI signal ENUM# is allowed to generate a hotswap event which will generate an interrupt (if the watchdog interrupt is also disabled). If 0, no hotswap events are signaled. Power up and reset state: 0.

ENEV — Read only bit that indicates a hotswap (ENUM#) event occurred. A high indicates a hotswap event occurred. Any write to I/O locations 8150-815Fh will reset this bit. Power up and reset state: 0.

WDEV — Read only bit that indicates a watchdog event occurred. A high indicates a watchdog event occurred. Any write to I/O locations 8150-815Fh will reset this bit. Power up state: 0. Reset state: the state of the bit before reset.

WDIE — If set, this bit causes a warm reset on a watchdog event. If reset, this bit causes an interrupt on a watchdog event. Power up and reset state: 0.

WDTV — Watchdog timer value. If not disabled, the watchdog timer is allowed to generate a watchdog event which will generate an interrupt or a warm reset depending on the state of the WDIE bit. If disabled, no watchdog events are signaled. A write to this register setting the timer length to a value (other than the disabled setting) will reset the watchdog counter to zero so that an inadvertent watchdog event does not occur sooner than expected after enabling the watchdog timer. This field produces the following time-out values:

Bit 1, Bit 0	Watchdog Timer Length
0,0	Disabled
0,1	8.2 seconds
1,0	128 ms
1,1	1.02 seconds

Notes: A write of the this register has a side effect of resetting the watchdog timer and the watchdog event indication register (bit 3) and the hotswap indication register (bit 4). Please refer to the Watchdog Timer section of *Chapter 4, Theory of Operation* for more information about the watchdog timer.

If you are using the watchdog timer, it is required to write to this register within the defined period of the timer to prevent generating either an interrupt or a warm reset.

Appendix B - Interrupts

Interrupt	Source
IRQ0	Timer
IRQ1	Keyboard Controller
IRQ2	Cascade Interrupt Input
IRQ3	COM B, COM A, or Unassigned
IRQ4	COM A, COM B, or Unassigned
IRQ5	Unassigned
IRQ6	Floppy Disk or Unassigned
IRQ7	LPT1: or Unassigned
IRQ8	Real Time Clock
IRQ9	Watchdog Timer
IRQ10	Unassigned
IRQ11	Unassigned
IRQ12	PS/2 Mouse
IRQ13	Floating Point Unit
IRQ14	Primary IDE
IRQ15	Secondary IDE
NMI	ISAbus IOCCHK/Memory Parity Error
SMI	Power Management/ECC/USB

Appendix C - Connectors and Jumpers

Introduction

This section details the connectors and jumpers used by the EPC-100 and gives the signal pinout of each connector.

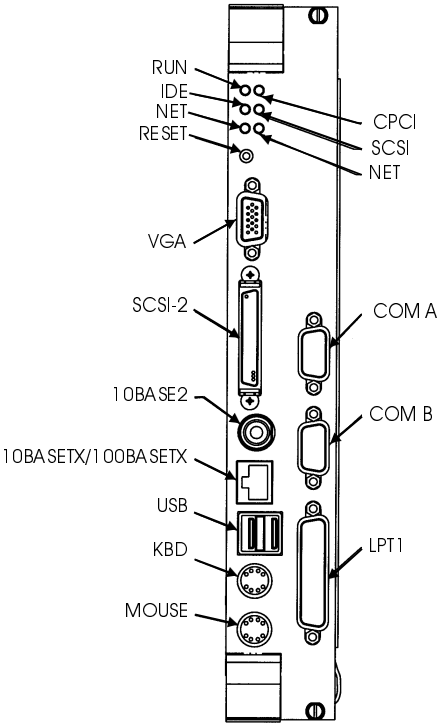


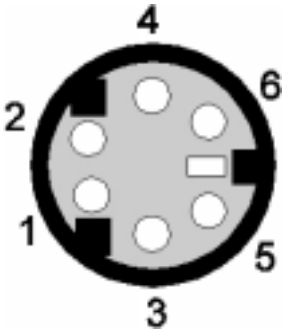
Figure C-1. EPC-100 Front Panel Connectors.

Keyboard Connector

The PS/2 keyboard connector is a 6-pin mini-DIN connector defined as follows:

Pin	Signal	Pin	Signal
1	Data	4	+5V
2	not used	5	Clock
3	Ground	6	not used

Table C-1. Keyboard Pin-Out.

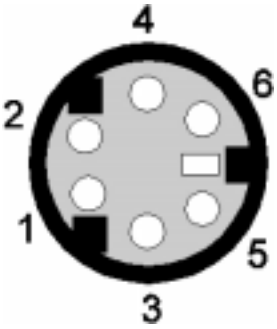


Mouse Connector

The PS/2 mouse connector is a 6-pin mini-DIN connector defined as follows:

Pin	Signal	Pin	Signal
1	Data	4	+5V
2	not used	5	Clock
3	Ground	6	not used

Table C-2. Mouse Pin-Out.



RS-232 Ports (COM A, COM B)

The RS-232 serial port male DB-9 DTE connectors are defined as follows:

Pin	Signal	Pin	Signal
1	Carrier detect	6	Data set ready
2	Receive data	7	Request to send
3	Transmit data	8	Clear to send
4	Data terminal ready	9	Ring indicator
5	Signal Ground		

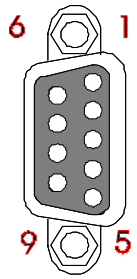


Table C-3. DB-9 Pin-Out.

Parallel Port

The LPT1 parallel port is an IEEE1284 EPC/EPP bi-directional female DB-25 connector defined as follows:

Pin	Signal	Pin	Signal
1	Strobe	14	Auto line feed
2	DB0	15	Error
3	DB1	16	Initialize printer
4	DB2	17	Select in
5	DB3	18	Signal ground
6	DB4	19	Signal ground
7	DB5	20	Signal ground
8	DB6	21	Signal ground
9	DB7	22	Signal Ground
10	Acknowledge	23	Signal ground
11	Busy	24	Signal ground
12	Paper End	25	Signal ground
13	Select		

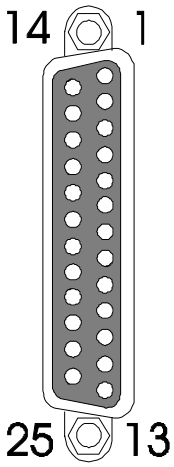


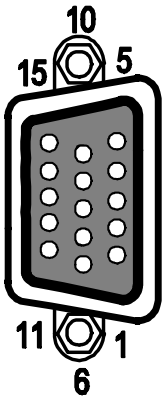
Table C-4. DB-25 Pin-Out.

SVGA Connector

The SVGA monitor port is a DB-15 connector defined as follows:

Pin	Signal	Pin	Signal
1	Red	9	(key)
2	Green	10	Ground
3	Blue	11	(not used)
4	(not used)	12	(not used)
5	Ground	13	Horizontal sync
6	Ground	14	Vertical sync
7	Ground	15	programmable output
8	Ground		

Table C-5. DB-15 Pin-Out.

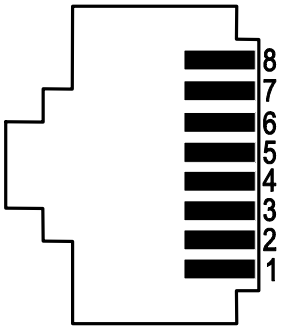


RJ45 Connector

The DTE RJ45 phone jack that supplies the 10Base-TX/100Base-TX interface to the Ethernet controller is defined as follows:

Pin	Signal
1	Tx+
2	Tx-
3	Rx-
4	No connect
5	No connect
6	Rx+
7	No connect
8	No connect

Table C-6. RJ45 Phone Jack Pin-Out.

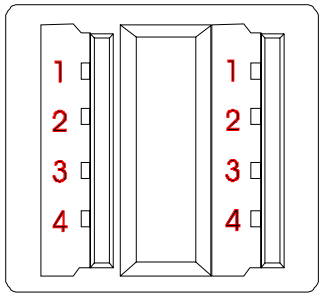


Dual USB Connector

The USB (Universal Serial Bus) connector is a dual, stacked 4-pin connector defined as follows:

Pin	Description
Mechanical Solder Lug	Shield Ground
1	VCC (1Amp Fused)
2	DATA-
3	DATA+
4	Signal Ground
Mechanical Solder Lug	Shield Ground

Table C-7. Dual USB Connector



SCSI-2 Connector

The SCSI-2 port is a female 50-conductor .050 center mini-D style connector defined in the following table. To disable the SCSI terminator, see *SCSI Terminator Disable Jumper*, later in this appendix.

Pin	Signal	Pin	Signal
1	Signal GND	2	~DB0
3	Signal GND	4	~DB1
5	Signal GND	6	~DB2
7	Signal GND	8	~DB3
9	Signal GND	10	~DB4
11	Signal GND	12	~DB5
13	Signal GND	14	~DB6
15	Signal GND	16	~DB7
17	Signal GND	18	~DBP
19	Signal GND	20	Signal GND
21	Signal GND	22	Signal GND
23	Signal GND	24	Signal GND
25	NC	26	Terminator Power
27	Signal GND	28	Signal GND
29	Signal GND	30	Signal GND
31	Signal GND	32	~ATN
33	Signal GND	34	Signal GND
35	Signal GND	36	~BSY
37	Signal GND	38	~ACK
39	Signal GND	40	~RST
41	Signal GND	42	~MSG
43	Signal GND	44	~SEL
45	Signal GND	46	~C/D
47	Signal GND	48	~REQ
49	Signal GND	50	~I/O

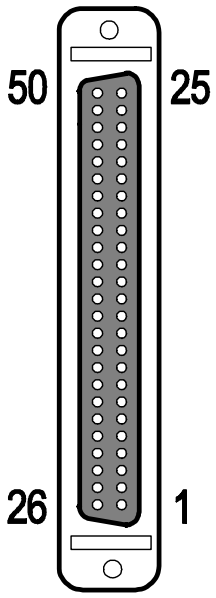


Table C-8. SCSI-2 Connector

EIDE (Primary) Connector

The Primary EIDE Connector is a male 44-pin right-angle header. If an optional hard disk drive is installed, it is installed on the primary channel. A slave drive may be attached also using a ribbon cable (user supplied). The optional hard disk is 2.5" style using power supplied by pins 41-44 of the connector. If you wish to connect a 40-pin connector, omit these power supply lines. The pins and signals are defined in the following table:

Pin	Signal	Pin	Signal
1	~RST	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	N.C.
21	DRQ	22	GND
23	~IOW	24	GND
25	~IOR	26	GND
27	IORDY	28	PPU
29	~DAK	30	GND
31	IRQ	32	IOCS16
33	A1	34	N.C.
35	A0	36	A2
37	~CS0	38	~CS1
39	ACT	40	GND
41	Vcc	42	Vcc
43	GND	44	GND

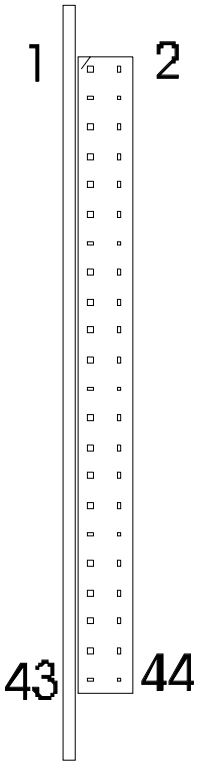
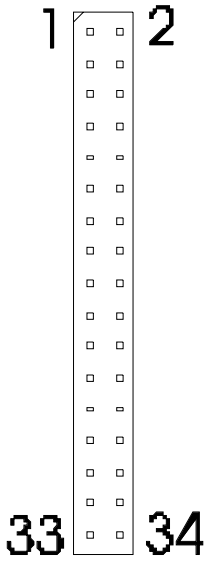


Table C-9. Primary EIDE Connector

Floppy Disk Drive Connector

The Floppy disk drive connector is a male 34-pin. The pins and signals are defined in the following table:

Pin	Signal	Pin	Signal
1	GND	2	DENSEL
3	N.C.	4	N.C.
5	N.C.	6	RATE0
7	Vcc*	8	INDEX
9	Vcc*	10	MTR1
11	Vcc*	12	DS0
13	GND	14	DS1
15	GND	16	MTR0
17	GND	18	DIR
19	GND	20	STEP
21	GND	22	WDATA
23	GND	24	WGATE
25	GND	26	TRK0
27	GND	28	WRPRT
29	GND	30	RDATA
31	GND	32	HDSEL
33	GND	34	DSKCHG



* - Vcc if jumper JP2 is installed (RadiSys floppy drive)
N.C. if jumper JP2 is not installed.

Table C-11. Floppy Disk Drive Connector.

CompactPCI J1 & J2 Connectors

The CompactPCI J1connector is a female 2mm-pitch 6 column by 25 row right angle Hard Metric (HM) connector. The CompactPCI J2 connector is exactly the same as the J1 connector except there are only 22 rows numbered 26-47. All of these signals have the standard CompactPCI revision 1.0 bus definitions. The symbol * before or after a signal indicates a note exists for this signal on the next page.

CompactPCI J1 Connector*						
Pin	A	B	C	D	E	F
1	**5V**	**-12V**	TRST#	**+12V**	**5V**	GND
2	TCK	**5V**	TMS	TDO	TDI	GND
3	INTA#	INTB#	INTC#	**5V**	INTD#	GND
4	BRSV	**GND**	**V(I/O)**	INTP	INTS	GND
5	BRSV	BRSV	RST#	**GND**	GNT0#	GND
6	REQ0#	**GND**	**3.3V**	CLK	AD[31]	GND
7	AD[30]	AD[29]	AD[28]	**GND**	AD[27]	GND
8	AD[26]	**GND**	**V(I/O)**	AD[25]	AD[24]	GND
9	C/BE[3]#	IDSEL	AD[23]	**GND**	AD[22]	GND
10	AD[21]	**GND**	**3.3V**	AD[20]	AD[19]	GND
11	AD[18]	AD[17]	AD[16]	**GND**	C/BE[2]#	GND
12-14	**Key Area**					
15	**3.3V**	FRAME#	IRDY#	**GND***	TRDY#	GND
16	DEVSEL#	**GND**	**V(I/O)**×	STOP#	LOCK#	GND
17	**3.3V**	SDONE	SBO#	**GND**	PERR#	GND
18	SERR#	**GND**	**3.3V**	PAR	C/BE[1]#	GND
19	**3.3V**	AD[15]	AD[14]	**GND**	AD[13]	GND
20	AD[12]	**GND**	**V(I/O)**	AD[11]	AD[10]	GND

Connectors

CompactPCI J1 Connector*						
Pin	A	B	C	D	E	F
21	**3.3V**	AD[9]	AD[8]	M66EN*	C/BE[0]#	GND
22	AD[7]	**GND**	**3.3V**	AD[6]	AD[5]	GND
23	**3.3V**	AD[4]	AD[3]	**5V**	AD[2]	GND
24	AD[1]	**5V**	**V(I/O)**	AD[0]	ACK64#	GND
25	**5V**	REQ64#	BRSV	**3.3V**	**5V**	GND

CompactPCI J2 Connector*						
Pin	A	B	C	D	E	F
26*	CLK1	**GND**	REQ1#	GNT1#	REQ2#	GND
27*	CLK2	CLK3	*SYSEN#	GNT2#	REQ3#	GND
28*	CLK4	**GND**	GNT3#	REQ4#	GNT4#	GND
29	**V(I/O)**	BRSV	C/BE[7]#	**GND**	C/BE[6]#	GND
30	C/BE[5]#	**GND**	**V(I/O)**	C/BE[4]#	PAR64	GND
31	AD[63]	AD[62]	AD[61]	**GND**	AD[60]	GND
32	AD[59]	**GND**	**V(I/O)**	AD[58]	AD[57]	GND
33	AD[56]	AD[55]	AD[54]	**GND**	AD[53]	GND
34	AD[52]	**GND**	**V(I/O)**	AD[51]	AD[50]	GND
35	AD[49]	AD[48]	AD[47]	**GND**	AD[46]	GND
36	AD[45]	**GND**	**V(I/O)**	AD[44]	AD[43]	GND
37	AD[42]	AD[41]	AD[40]	**GND**	AD[39]	GND
38	AD[38]	**GND**	**V(I/O)**	AD[37]	AD[36]	GND
39	AD[35]	AD[34]	AD[33]	**GND**	AD[32]	GND
40	BRSV	**GND**	FAL#	*REQ5#	*GNT5#	GND
41	BRSV	BRSV	DEG#	**GND**	BRSV	GND
42	BRSV	**GND**	PRST#	*REQ6#	*GNT6#	GND
43	USR	USR	USR	USR	USR	GND

Connectors

CompactPCI J2 Connector*						
Pin	A	B	C	D	E	F
44	USR	USR	USR	USR	USR	GND
45	USR	USR	USR	USR	USR	GND
46	USR	USR	USR	USR	USR	GND
47	USR	USR	USR	USR	USR	GND

× **Notes:**

1. This diagram defines the pinout from the front of the system chassis. All pins are medium length (level 2) except C16 and D15 which are long (level 3) and short (level 1), respectively. The V(I/O) signals are either 5V or 3.3V, depending on the system implementation.
2. Pin D15 (short, level 1) is used as BD_SEL# for hot-swap capable boards.
3. Pin C16 (long, level 3) is used for early power to hot-swap capable boards for controlling the buffer logic.
4. Pin D21 is defined as GND for 33MHz backplanes. Use of this signal in 66MHz systems will be as a bussed signal to all slots.
5. Rows 26-28 are only implemented on the system board.
6. C27 is grounded at the system slot only. Remaining slots leave C27 unconnected.
7. System slot adapters that do not support seven REQ#/GNT# signals must provide a mechanism to connect any of the Peripheral Slots 2-8 that may need arbitration service depending on the adapter installed.

Fan Failure Detect Enable Jumper

The Fan Failure Detect Enable Jumper, labelled Fail Fail Conn, is located at the bottom of the Main board, behind the front panel mouse connector as shown in Figure C-1. The jumper is installed to enable detection of fan failure during POST.

SCSI Terminator Disable Jumper

The SCSI Terminator Disable Jumper is located behind the top ejector on the Main board. To disable the SCSI terminator, apply a jumper. The last module in a SCSI chain must have an active terminator, while all other modules must have the terminator disabled. The EPC-100 is shipped with the jumper removed, enabling the SCSI terminator.

Floppy Power Jumper

To accommodate different floppy disk drives, a jumper is provided to enable/disable power from the floppy drive connector to the floppy cable and the floppy disk drive to which it is connected. Labelled P10 Floppy Pwr Conn, this jumper is located near the middle of the back edge of the main circuit board, immediately in front of the floppy drive connector. When this jumper is installed, power to the floppy cable is enabled. When this jumper is removed, power to the floppy cable is disabled. The default factory setting is installed, enabling power to the floppy drive cable.

Appendix D - Error Messages

Introduction

Boot Failures

The System BIOS attempts to display an error message on the VGA and halts when it encounters the following error conditions:

1. Fixed disk error
    - No drive connected
    - Configured for 0 cylinders
    - Controller reset failed
    - Drive not ready
    - Track 0 seek timed out
    - Drive initialization failed
    - Drive recalibration failed
    - Last track seek failed
2. Video error
    - Color/Mono switch not set correctly
3. Timer error
    - System timer (0) failed
4. Diskette error
    - Floppy type does not match setup

5. I/O chip error
    - I/O conflicts exist for serial and parallel ports, floppy, hard disk (any or all)
6. Other error
    - IRQ conflict, unsupported COM port configuration, keyboard locked
    - Pentium™ cooling fan has failed

The System BIOS *prints* an error message *but does not halt* when it encounters the following error conditions:

1. Keyboard error
    - Keyboard reset failed
    - Keyboard not found
    - Keyboard interrupts failed
    - RTC error
    - RTC lost power
    - CMOS error
    - RTC battery failed
    - CMOS checksum failed
2. Configuration error
    - Previous POST execution was incomplete
    - User BIOS Extension Region X exceeds DFFFFh